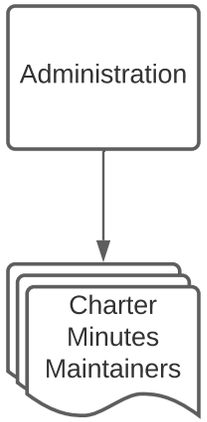
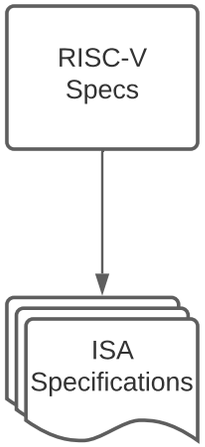
RISC-V GitHub Structure 2021

github.com/riscv-admin



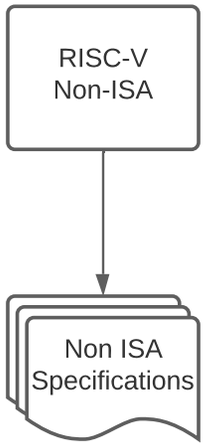
marketing
Software List
Cores List
Educational Materials
Getting Started Guides
Governance
Community
Groups (e.g. RAS)
riscv-code-speed-optimization
etc...

github.com/riscv



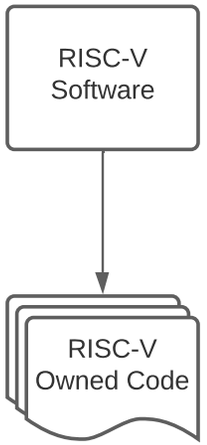
Priv
UnPriv
Virt Mem
bitmanip
P Spec
fast-int
zfinx
crypto
j ext
Vector
Alt FP
Opcodes
CMOs
sail-riscv
Code Size Reduction
Platform Specs
PLIC

github.com/riscv-non-isa



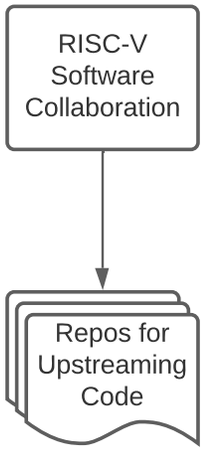
Overlay
rvv-intrinsic-doc
riscv-sbi-doc
riscv-elf-psabi-doc
riscv-debug-spec?
riscv-toolchain-conventions
riscv-toolchains-runtimes
config struct?
RASD
Trace
Nexus
riscv-c-api-doc
riscv-eabi-spec
riscv-asm-manual
Arch Tests
Arch Tests Reports

github.com/riscv-software-src



riscv-pk
OpenSBI
meta-riscv
riscv-tests
homebrew
riscv-openOCD
riscv-isac
riscv-ctg
Config Validator
SIG/HC/TG Code
-> riscv-embedded-sig
-> riscv-technology-hc
riscv-ovpsim pointer
riscv-isa-sim

github.com/riscv-collab



riscv-edk2
riscv-edk2-platforms
riscv-uefi-edk2-docs
gcc
v8
binutils
gnu-toolchain
glibc
newlib