Technical Newsletter
2023-09-29
Volume: I

News from HCs, ICs,TGs and SIGs

Privileged Spec IC

Smctr/Ssctr - Control Transfer Records Internal Review Underway

The CTR Technical Group has completed the initial stable specification for the Smctr/Ssctr ISA extensions. It is currently undergoing a 2-week internal review, set to conclude on October 5th. The specification is available here.

Smcsrind/Sscsrind - Indirect CSR Access Approved by ARC

The "Indirect CSR Access (Smcsrind/Sscsrind)" ISA extension has received approval from the ARC (Architecture Review Committee) to freeze. The specification is available here.

Unprivileged Spec IC

A case for byte and halfword AMO

A new proposal for adding byte and halfword atomic memory operations to the Unprivileged ISA (Unpriv IC) has been tabled. The proposal aims to enhance the architecture's granularity for atomic operations. Review the proposal here and join the ongoing discussion thread to share your insights.

A case for ssamoswap

A query regarding the necessity of the ssamoswap instruction was raised in the AR review for Zicfiss (shadow stack for control flow integrity) extensions. To address this, the TG has compiled a paper elaborating the case for ssamoswap. Check out the paper here for an in-depth look.

Zimop/Zcmop - Specification for Internal Review

The RISC-V Fast Track "Maybe Ops" extensions (Zimop/Zcmop) specification has been posted for internal review on September 124, 2023 to the tech-announce mailing list. The review ends on October 8, 2023. See the announcement post (link) for details on how to participate in the review.

Security HC

Adding supervisor domain IDs to PMPs

A proposal to add supervisor domain IDs to PMPs to potentially reducing microarchitectural flushing is being discussed in the Smmtt task group. See riscv/riscv-smmtt#3.

Add supervisor domain support to AIA/APLIC to contain interrupt handling to a domain

A proposal to add supervisor domains to interrupt handling in AIA and APLIC is being discussed in the Smmtt TG. Discussion here: riscv/riscv-smmtt#5.

CoVE-IO - Initial ABI and flows for the Confidential VM IO extensions are defined

The initial flows and their supporting ABIs for the confidential supervisor domain manager (a.k.a the TSM) to establish a secure connection with TEE-IO devices have been approved and merged. The TSM will use this secured connection to assign physical devices interfaces to confidential VMs.

Smmtt - Supervisor Domains Specification Updates

The Smmtt TG in the Security HC (Trusted Computing SIG) received approval of the ratification plan at tech chairs. The TG has been actively working on a Supervisor Domains Access Protection specification to support flexible physical memory isolation between Supervisor (and Hypervisor) Domains. Typically, there is a single supervisor domain of execution with access to all physical memory. Supervisor Domain Access Protection, is a RISC-V privileged architecture extension to support flexible physical address space isolation for more than one supervisor domain. Supervisor domains enable trusted execution use cases for RISC-V platforms e.g. Confidential VM Extension (CoVE), TEE Security Services, Secure Devices (CoVE-IO) etc.

SOC Infrastructure HC

RAS Error Record Interface (RERI) Specification Plan was Approved

The RAS ERI Specification Plan was Approved in the Tech Chairs meeting on Sep 20th, 2023. The plan can be found here.

News From the CTO Office

Zfa and Vector Crypto were Ratified by the Board of Directors

By Mark Himelstein, CTO, RISC-V International:

The Board of Directors (BOD) ratified both Zfa and Vector Crypto on Sep 28th 2023.

The dedication and effort put forth by the Owners, Authors, Technical Groups, and the wider community have been truly remarkable.

Special gratitude goes to Andrew Waterman for his contributions to Zfa and to Ken Dockser and Rich Newell for their work on Vector Crypto. Thanks to everyone else who played a pivotal role in achieving this milestone.

Elections

2023 TSC Chair and Vice-chair Election

Greg Favor (Ventana) has been elected as the new TSC Chair and Philipp Tomsich (Vrull) as the new TSC Vice-chair. Congratulations to both!

2023 TSC Strategic Member Election

The 2023 TSC Strategic Member Election is underway and will conclude on Thursday, October 5, 2023.

Familiarize yourself with the nominees (sorted alphabetically) and make your voice heard:

- David Weaver, Akeana.
- Hualin Wu, Terapines Technology.
- Ken Dockser, Tenstorrent.
- Liuxi Yang, Sophgo Technologies.
- Roger Espasa, Semidynamics.

2023 TSC Community/Individual Member Election

The 2023 TSC Community/Individual Member Election is underway and will conclude on Thursday, October 5, 2023.

Familiarize yourself with the nominees (sorted alphabetically) and make your voice heard:

- Guy Lemieux, Individual Member.
- Nick Kosifidis, FORTH.

Election Notes

Should you be uncertain about your company's designated Voting Contact, please reach out to info@riscv.org, and we will assist you in identifying your official voting member.

For any other queries, or if your ballot hasn't reached you, kindly email help@riscv.org.

DevPartner 10xEngineering Completed Work on Atomics Architecture Test

The RISC-V Development Partner 10xEngineers completed work on Architecture Tests for the Atomics extensions. For more information, see PR#257 in the in the riscv-arch-test repo and PR#69 in the riscv-ctg repo.

Calendar in your own timezone

The RISC-V Technical calendar is now automatically available in your own timezone. To view the calendar in your own timezone, click on the link.

Where to Send Internal and Public Review Requests?

We recently received inquiries about the appropriate channels to submit specifications for both internal and public reviews. To ensure clarity and consistency for everyone, please note the following:

- Internal Review: send to tech-announce.
- Public Review: send to both tech-announce and isa-dev.

Etherpad

We're piloting Etherpad to enhance our note-taking during meetings. Etherpad is a real-time, browser-based editor where users can co-edit documents instantly. No login needed – simply create a pad and begin. Afterwards, export your notes to platforms like GitHub or Google Docs. Etherpad should not store permanent content. To access Etherpad, click on the link. Pads are reusable, so feel free to use the same pad for multiple meetings.

Jira and GitHub Access

To ensure a seamless experience with RISC-V International's tools and platforms, please first verify your access to Groups.io, GitHub, and Jira by clicking on the following Verify Access.

If you encounter any issues or do not have the necessary permissions, kindly reach out to us by sending an email to help@riscv.org.

Upcoming Events

- RISC-V Summit North America: November 7-8, 2023, Santa Clara, CA, USA. Schedule is live! Register today.

Newsletter Contributions

To submit a topic for our newsletter, click here. Be sure to carefully read the submission guidelines!

Contact Information

For any queries, visit our help.riscv.org or email us at help@riscv.org.

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