Technical Newsletter
2023-10-13
Volume: 3

News from HCs, ICs,TGs and SIGs

Privileged Spec IC

Smctr, Ssctr - Control Transfer Records (CTR)

Control Transfer Records (CTR) spec completed internal review. Review feedback has been incorporated into the stable v0.5 spec release. The specification developers anticipate submitting the specification for ARC review later this month, seeking their approval to Freeze the specification. You can track the specification's progress here: RVS-973.

Unprivileged Spec IC

Zacas - Atomic Compare-and-Swap

The proposed extension for Atomic Compare-and-Swap (CAS) instructions, known as Zacas, has successfully concluded its public review process. The Public Review comments can be found here. The Zacas IC is now in the process of incorporating any necessary feedback and will complete the Ratification-Ready steps.

Zabha - Byte and Halfword Atomics

The Fast Track extension Zabha received formal approval for its plan during the most recent Chairs meeting on October 11th, 2023. To learn more about the plan, you can access the details here. Additionally, you can track its ongoing progress by visiting this link.

CoVE-IO - Confidential VM Extensions for IO

The plan for the specification CoVE-IO has been approved during the last Chairs meeting on October 11th, 2023. To learn more about the plan, you can access the details here. Additionally, you can track its ongoing progress by visiting this link.

Initial discussions about memory tagging have started

Initial discussions about memory tagging have kicked off in the Runtime Integrity SIG and J Extension TG group meetings. Several proposals [1, 2] have been discussed. A draft rationale doc for pre-review by the architecture review committee is being crafted that summarizes motivation and use cases.

SOC Infrastructure HC

Server SoC Specification

The Server System-on-Chip (SoC) Technical Group (TG) has put together a comprehensive specification outlining the standardized hardware capabilities that portable system software, including operating systems and hypervisors, can depend on within a RISC-V server SoC. We invite you to read the document and join the ensuing discussion to provide valuable insights before we finalize the spec. Your feedback is crucial at this stage.

DTPM Special Interest Group

Recent developments within this SIG include:

- The E-Trace Encapsulation TG has successfully completed a draft specification, which is nearly ready for review. Ratification plan in the works.
- The draft for the E-Trace specification 2.0.1 is also close to complete. This is an editorial, non-normative update covering a few clarification and corrections, and also replaces control field definitions with cross references to the Common Control Spec developed under the auspices of the N-Trace TG.
- The process of establishing a new Secure External Debug TG, which promises to bring innovative insights and advancements to our endeavors, has begun.

Application & Tools HC

Recent updates to the riscv-gnu-toolchain repository brought the integration of GCC 13.2, LLVM 17.0.2, QEMU 8.1.1, and newlib 4.3.0. The riscv-gnu-toolchain repo helps to build RISC-V cross-toolchains for RV32 and RV64 for both, embedded targets (newlib, musl) and Linux systems (glibc). Despite its name, the repository also supports building LLVM-based toolchains since June this year.

News From the CTO Office

Voting

Technical Steering Committee Votes

- Technical Steering Committee Vote to Approve the E-Trace Encapsulation Task Group is underway, the **end date is Oct 16th**. The voting text can be found here.
- Technical Steering Committee Vote to Approve the PQC Task Group is underway, the **end date is Oct 24th**. The voting text can be found here.
- Technical Steering Committee Vote to Approve the Server SOC Task Group is underway, the **end date is Oct 25th**. The voting text can be found here.
- TSC Approval for sending the Counter Mode Filtering Fast Track Ext to the Board for Ratification is underway, the **end date is Oct 26th**.The voting text can be found here.

Committee Chair Votes

- Ratification-Ready Milestone vote for Compare and Swap Fast Track is underway, the **end date is Oct 18th**. The voting text can be found here.
- Ratification-Ready Milestone vote for Svadu Fast Track is underway, the **end date is Oct 19th**. The voting text can be found here.
- Freeze Milestone vote for BFloat16 Fast Track is underway, the **end date is Oct 25th**. The voting text can be found here.

Technical Resources

Calendar in your own timezone

The RISC-V Technical calendar is now automatically available in your own timezone. To view the calendar in your own timezone, click on the link.

Etherpad

We're piloting Etherpad to enhance our note-taking during meetings. Etherpad is a real-time, browser-based editor where users can co-edit documents instantly. No login needed – simply create a pad and begin. Afterwards, export your notes to platforms like GitHub or Google Docs. Etherpad should not store permanent content. To access Etherpad, click on the link. Pads are reusable, so feel free to use the same pad for multiple meetings.

Jira and GitHub Access

To ensure a seamless experience with RISC-V International's tools and platforms, please first verify your access to Groups.io, GitHub, and Jira by clicking on the following Verify Access.

If you encounter any issues or do not have the necessary permissions, kindly reach out to us by sending an email to help@riscv.org.

Upcoming Events

- RISC-V Summit North America: November 7-8, 2023, Santa Clara, CA, USA. Schedule is live! Register today.

Newsletter Contributions

To submit a topic for our newsletter, click here. Be sure to carefully read the submission guidelines!

Contact Information

For any queries, visit our help.riscv.org or email us at help@riscv.org.

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