



Technical Newsletter

2023-11-03

Volume: 4

News from HCs, ICs, TGs and SIGs

Profiles & Platforms

Profiles TG discussion of keeping vs. dropping support for C extension and halfword-aligned (16/32/48/64-bit) instructions in *all* Application-class profiles (RVA, RVB)

The Profiles Task Group is having an ongoing discussion with Qualcomm regarding a proposal to drop IALIGN=16 from the RVA and RVB profiles. This proposal drops the C extension (and follow-on 16-bit extensions such as Zcb), disallows future 48-bit instructions, and requires future 64-bit instructions to be 64-bit-aligned.

The discussions have also included discussion of introducing new ARM-like 32-bit instructions using the existing C encoding space (as well as use of this encoding space for other future instructions). All such new ISA extensions would only be available to designs that don't support the C extension (e.g. not RV64GC designs).

Various slide sets for and against have been presented, with more to come. For/against arguments include considerations of design complexity, static and dynamic code size reduction, instruction count reduction, performance benefit and/or impact, fusing simple instructions and cracking new "complex" instructions, dropping backward compatibility with existing RVA profiles, and software ecosystem impacts (especially those markets with components of binary software distribution, i.e. Android and Linux distributions), as well as other factors.

The material presented by Qualcomm can be found in the links below:

- [Qualcomm's initial proposal](#)
- [A response to Qualcomm's proposal that argues IALIGN=16 should be retained](#)
- [Qualcomm's rebuttal](#)
- [Qualcomm's data on Android Compression of C vs. Zics](#)

Join the [Mailing List](#) to participate in the discussion. Attend the [meetings](#).

Server Platform Task Group

The Server Platform Task Group, dedicated to creating a versatile server platform compatible with various Linux Distributions and other relevant operating systems, is at inception. This group will report directly to the Technical Steering Committee to ensure its work aligns closely with our community's needs, promising significant and direct impact.

- **Acting Chair:** Andrei Warkentin (Intel)
- **Acting Vice-Chair:** John Ronco (SiFive)
- [Mailing List](#)
- [Charter](#)

Unprivileged Spec IC

BFloat16 Fast Track ISA Specification Freezes

The [BFloat16](#) Fast Track ISA specification was approved by the Committee Chairs as having completed the Freeze milestone on October 25, 2023. It should be entering Public Review soon.

Attached Matrix Facility (AMF) Extension Task Group

The Attached Matrix Facility (AMF) Extension Task Group is in inception. The proposed Task Group will report directly to the Unprivileged IC and "dotted line" to the Applications & Tools HC. The Attached Matrix Facility (AMF) Task Group is tasked with specifying an extension to the RISC-V ISA that implements a scalable (i.e., with the ability to operate on different operand sizes and allow the writing of matrix-geometry agnostic code) matrix operations unit. This matrix operations unit will be a standalone block implementable without dependencies on the RISC-V Vector extension.

- **Acting Chair:** Chou Jing (Alibaba)
- **Acting Vice-Chair:** Philipp Tomsich (VRULL)
- [Mailing List](#)
- [Charter](#)

High Assurance Cryptography Task Group Call for Candidates

The Unprivileged ISA Committee and the Security Horizontal Committee have announced the Call for Candidates for the forming High Assurance Cryptography Task Group. This call closes on November 6, 2023. More information about the call and how to submit a nomination, please see the [announcement](#).

Privileged Software HC

Public Review of the Supervisor Binary Interface (SBI)

The [Supervisor Binary Interface \(SBI\) version 2.0](#) public review ends on November 6, 2023. For more information on the review and details of how to participate, please see the review announcement on [isa-dev](#).

Public Review of Advanced Configuration and Power Interface - Functional Fixed Hardware (ACPI FFH)

The [Advanced Configuration and Power Interface - Functional Fixed Hardware \(ACPI FFH\)](#) public review ends on November 6, 2023. For more information on the review and details of how to participate, please see the review announcement on [isa-dev](#).

SOC Infrastructure HC

Server SOC Task Group

The Server SOC Task Group was approved by TSC. It shall define a specification for a standardized set of hardware capabilities that portable system software such as operating systems and hypervisors can rely on being present in a RISC-V server SoC.

- **Chair:** Ved Shanbhogue (Rivos Inc.)
- **Vice-Chair:** Dr. Xie Shaolin (Alibaba)
- [Mailing List](#)
- [Charter](#)

E-Trace Encapsulation Task Group

The E-Trace Encapsulation Task Group was approved by TSC. It will define how trace packet payloads shall be encapsulated.

- **Chair:** Iain Robertson (Siemens)
- **Vice-Chair:** Paul Donahue (Ventana Micro Systems)
- [Mailing List](#)
- [Charter](#)

Security HC

CoVE-IO Attestation Stages

The initial models for CoVE-IO attestation are now defined in the [Attestation section](#). Both local and remote flows for attesting to assigned devices are supported.

Post Quantum Cryptography Task Group

The Post Quantum Cryptography Task Group was approved by TSC. It will explore, recommend, and develop RISC-V Instruction Set Architecture (ISA) Extensions that enhance performance and implementation efficiency for contemporary public-key cryptography, with a focus on standard Post-Quantum Cryptography algorithms.

- **Chair:** Markku-Juhani O. Saarinen (Tampere University)
- **Vice-Chair:** Nicolas Brunie, SiFive (SiFive)
- [Mailing List](#)
- [Charter](#)

Technology HC

Composable Extensions (CX)

The SoftCPU SIG is finalizing a charter to create a new TG for the Composable Extensions (CX) extension. CX is a framework that will enable robust composition of multiple independently authored custom ISA extensions, including legacy custom extensions, so they may be assembled in a conflict-free way into a target RISC-V implementation. By multiplexing the custom opcode space, CX will provide features such as naming and versioning, discovery, hardware module reuse, state context management, and stable software binaries that don't need recompilation for each target system — all without a central management authority. The SIG will have an in-person meeting at the upcoming RISC-V Summit on Member's day (Monday 6 November) at 10:30am in room 202.

ISA Infrastructure HC

SAIL

Vector extension support has been enabled in Sail model

The Sail model extension for RISC-V vector instructions has been merged into the main branch of the [sail-riscv](#) repository in a recent update. It is implemented by the developers from RIOS Lab and has been progressively reviewed in the form of multiple PRs. The final update as an integrated commit can be found [here](#).

News From the CTO Office

New Disclaimer Video

Mark Himmelstein, CTO of RISC-V International, has recorded the second version of RISC-V Meetings Disclaimer. You can find the video [here](#).

Voting

Technical Steering Committee Votes

- [TSC Vote for Approval of Adam Zabrocki as the Vice-chair of the J Extension Task Group](#). End date 11/7/2023.
- [TSC Approval Vote to send the Compare & Swap \(Zacas\) Fast Track Ext to the Board for Ratification](#). End date 11/9/2023.
- [TSC Approval Vote for sending the Svadu Fast Track Extension to the Board for Ratification](#). End date 11/10/2023.
- [TSC Approval Vote for sending the Conditional Ops Fast Track Extension to the Board for Ratification](#). End date 11/15/2023.

Committee Chair Votes

- [Freeze Milestone for May-Be-Ops Fast Track Specification Committee Chair Sign Off](#). End date 11/10/2023.
- [Freeze Milestone for Indirect CSR Access Fast Track Extension Committee Chair Sign Off](#). 11/6/2023.

Technical Resources

Calendar in your own timezone

The RISC-V Technical calendar is now automatically available in your own timezone. To view the calendar in your own timezone, click on the [link](#).

Etherpad

We're piloting Etherpad to enhance our note-taking during meetings. Etherpad is a real-time, browser-based editor where users can co-edit documents instantly. No login needed – simply create a pad and begin. Afterwards, export your notes to platforms like GitHub or Google Docs. Etherpad should not store permanent content. To access Etherpad, click on the [link](#). Pads are reusable, so feel

free to use the same pad for multiple meetings.

Jira and GitHub Access

To ensure a seamless experience with RISC-V International's tools and platforms, please first verify your access to Groups.io, GitHub, and Jira by clicking on the following [Verify Access](#).

If you encounter any issues or do not have the necessary permissions, kindly reach out to us by sending an email to help@riscv.org.

Presentations

Discovering Faster Matrix Multiplication Algorithms with Reinforced Learning

Alhussein Fawzi from DeepMind presented about discovering faster matrix multiplication algorithms with reinforced learning. The recording can be found [here](#).

RISC-V Technical Session: Scalar, vector, matrix – the next stage in SIMD processing

José Moreira from IBM presented at the RISC-V Technical Session: Scalar, vector, matrix – the next stage in SIMD processing. The presentation can be found [here](#).

Upcoming Events

RISC-V Summit 2023

[RISC-V Summit North America](#): November 7-8, 2023, Santa Clara, CA, USA. [Schedule is live!](#) [Register today](#).

RISC-V Software Porting and Optimization Championship

The PLCT Lab has initiated the "RISC-V Software Porting and Optimization Championship" to draw developers to the RISC-V ecosystem and expedite its software development. The global competition emphasizes desktop and server software, spanning various categories like compilers, runtime environments, and AI software stacks. More details can be found in one of the following links:

- [Simplified Chinese](#)
- [English](#)

Call for Papers: Third International Workshop on RISC-V for HPC at HPC Asia

The Third International Workshop on RISC-V for HPC Workshop invites submissions of original research and work-in-progress related to RISC-V and its applications in High Performance Computing (HPC). Papers from both academia and industry are welcome. [The submission deadline is November 28, 2023](#).

Newsletter Contributions

To submit a topic for our newsletter, [click here](#). Be sure to carefully read the submission guidelines!

Contact Information

For any queries, visit our help.riscv.org or email us at help@riscv.org.

