**Technical Newsletter**
2023-11-17
**Volume: 5**

# News from TSC, ARC, ICs, HCs, SIGs and TGs

## Technical Steering Committee (TSC)

### Profiles & Platforms

As mentioned in the last newsletter, the Profiles TG has been discussing whether to keep C as mandatory in the RVA profiles (as well as other proposals related with C potentially being "dropped" from RVA profiles). As part of reviewing the status of this topic, the RVI BoD (in its in-person meeting last week) had its own discussions and ultimately voted and approved the necessity to continue keeping C as a mandate in RVA profiles. For a summary of the board's considerations and conclusions, read the announcement from the TSC Chair by clicking here.

## Unprivileged Spec IC

### New J Extension Vice-Chair

Adam Zabrocki, from NVIDIA, was confirmed as the new Vice-chair of the J-extension Task Group. Adam is very active in the RISC-V space and is a key member of NVIDIA's Offensive Research and RISC-V security team. Congratulations Adam!

## ISA Infrastructure HC

### SAIL

### Sail Model State of the Union

Bill McSpadden (RISC-V International) gave a presentation on the state of the RISC-V Sail model at the North America RISC-V Summit on Nov. 6, 2023 during Members' Day. The presentation centered on the slow pace of development (with an appeal for more contributors and reviewers), using Sail source code in specifications and the progress that has been made over the past year (including the merge of the vector implementation). You can find the slides here.

# News From the CTO Office

## Action Required for Chairs and Vice-Chairs: LFX and RISC-V Jira Account Creation

Please, read the following instructions carefully only if you are not able to access RISC-V Jira or has never accessed it before.

We are moving to Jira. In order to access RISC-V Jira, it is required to have a LFX account. If you do not have a LFX account, please create one by clicking here.

Once you have created your LFX account, please login in RISC-V Jira by clicking here.

In order to access the resources within RISC-V Jira, you will need to be added to the right group. Please open an issue at help.riscv.org and provide the following information: LFX email address and Jira username. We will add you to the right group and you will receive an email notification once you have been added.

If you **cannot** access help.riscv.org, please send an email to help@riscv.org with your GitHub ID so we can add you to the help repository.

# Voting

### Technical Steering Committee Votes

- TSC Vote to Approve the High Assurance Cryptography Task Group. End date 11/28/2023.
- TSC Vote for Approval of Anup Patel as the Chair of the Privileged Software Horizontal Committee. 11/28/2023.

# Technical Resources

### Calendar in your own timezone

The **RISC-V Technical Meetings Calendar** is available in your own timezone here.

### Etherpad

Etherpad, a real-time browser-based editor where users can co-edit documents instantly, is available. No login needed. Etherpad should not store permanent content. To access Etherpad, click on the here. Pads are reusable, so feel free to use the same pad for multiple meetings.

# News

## RISC-V Summit North America 2023

The photos from the Summit are now available for viewing! You can find a collection of great shots at this link. Enjoy browsing through them!

## DynamoRIO Adds Support for RISC-V

DynamoRIO is a versatile runtime code manipulation system enabling transformations on any part of a program during execution. It offers a comprehensive interface for creating dynamic tools for program analysis, profiling, optimization, and more. Unique in its ability to perform arbitrary modifications beyond simple callouts, it supports IA-32/AMD64/ARM/AArch64 instruction manipulation. Efficient and transparent, DynamoRIO works with unmodified applications on standard operating systems (Windows, Linux, Android) and hardware, with Mac OSX support underway.

This work was mainly done by LIU Yang (PLCT Lab, ISCAS) and Stanislaw Kardach (SemiHalf). Several developers and reviewers also contributed to the RISC-V backend. Many thanks to all of them!

# Upcoming Events

## RISC-V Summit Europe 2024

RISC-V Summit Europe: June 24-28, 2024, Munich, Germany.

# Glossary

- **TSC**: Technical Steering Committee
- **ARC**: Architecture Review Committee
- **IC**: ISA Committee
- **HC**: Horizontal Committee
- **SIG**: Special Interest Group
- **TG**: Task Group

# Newsletter Contributions

To submit a topic for our newsletter, click here. Be sure to carefully read the submission guidelines!

# Contact Information

For any queries, visit our help.riscv.org or email us at help@riscv.org.


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