News from TSC, ARC, ICs, HCs, SIGs and TGs

Unprivileged Spec IC

Updates from the Shadow Stack and Landing Pads Task Group

The Shadow Stack and Landing Pads Task Group (TG) is pleased to announce the successful completion of the architectural review for the Zicfilp extension, introducing labeled landing pads ISA for enhanced forward-edge control-flow integrity. Concurrently, the TG is actively collaborating with the ARC to address outstanding issues with the Zicfiss extension, which focuses on implementing shadow stacks ISA for reinforcing backward-edge control-flow integrity. The extension updates were discussed at the RISC-V mini-conference held at Linux Plumbers Conference 2023 (slide). We look forward to sharing further updates as our work progresses.

Security HC

RISC-V CoVE updates at Linux Plumbers Conference

A Confidential Computing Micro-Conference (MC) was held at the Linux Plumbers Conference (LPC 2023) on November 14th - See detailed agenda here. RISC-V CoVE updates were discussed as well - See slides here. Related topics of attestation standards was discussed (link). In addition to the Confidential computing MC, there was a proposal for a generalized ABI verbs for TEE-IO - see link - a follow on Birds-of-a-feather (BoF) was held for this topic - the CoVE-IO TG ABI will be one of the inputs towards this common ABI for Linux host and guest interfaces.

High-Assurance Cryptography Task Group Approved by TSC

The High-Assurance Cryptography Task Group was approved by TSC. It will explore, recommend, and develop RISC-V Instruction Set Architecture (ISA) Extensions that enhance performance and security for classical cryptographic algorithms like AES. The two main aspects considered are improved key management and the ability for micro-architectures to provide side-channel resistant implementations.
SOC Infrastructure HC

Updates from the Server SoC Task Group

The Server SoC Task Group (TG) is pleased to present the initial draft of the Server SoC Test Specification. This document is a key addition to the requirement specification draft previously developed by the TG. It details tests for a standardized set of hardware capabilities, essential for portable system software such as operating systems and hypervisors, in a RISC-V server SoC.

We strongly encourage your engagement in reviewing this draft, available here. Your expertise and feedback at this stage are invaluable and will significantly contribute to refining and finalizing the specification. Your insights are crucial in shaping the future of RISC-V server SoC development.
News From the CTO Office

Recently Ratified Specifications

In the latest Board of Directors meeting, held on Nov 30th 2023, the following specifications were ratified:

- Smcntrpmf - Counter Mode Filtering. Author: Beeman Strong (Rivos Inc.).
- Svdau - Hardware Updating of PTE A/D Bits. Author: Ved Shanbhogue (Rivos Inc.).
- Zicond - Conditional Operations. Author: Philipp Tomsich (VRULL).

New Meeting Schedule for 2024

Starting in January 2024, the RISC-V Technical Meetings will be reorganized to better serve the community. Time slots considering the weeks of the year (2024 will have 53 weeks: 27 odd and 26 even), were allocated for the following groups:

- Privileged IC, Unprivileged IC, ISA Infrastructure HC, Profiles.
- Privileged Software HC, Applications and Tools HC, Platforms.
- SOC Infrastructure HC.
- Security HC.
- Technology HC.
- Governance (TSC, Chairs, Technical Governance).

You can see a detailed breakdown of the time slots allocated as per the approved plan here.

Chairs and Vice-Chairs of SIGs and TGs are encouraged to work with their respective IC or HC in order to define the best time slot for their meetings. ICs and HCs Chairs and Vice-Chairs are also encouraged to work with their peers in order to accommodate all meetings in the best possible way.

Action Required for Chairs and Vice-Chairs: LFX and RISC-V Jira Account Creation

Please, read the following instructions carefully only if you are not able to access RISC-V Jira or has never accessed it before.

We are moving to Jira. In order to access RISC-V Jira, it is required to have a LFX account. If you do not have a LFX account, please create one by clicking here.
Once you have created your LFX account, please login in RISC-V Jira by clicking here.

In order to access the resources within RISC-V Jira, you will need to be added to the right group. Please open an issue at help.riscv.org and provide the following information: LFX email address and Jira username. We will add you to the right group and you will receive an email notification once you have been added.

If you cannot access help.riscv.org, please send an email to help@riscv.org with your GitHub ID so we can add you to the help repository.

Voting

Technical Steering Committee Votes

• Technical Steering Committee Vote to Approve the SmMTT Task Group. End date: 12/6/2023.

Committee Chair Votes

• Ratification-Ready Milestone for SBI 2.0 and ACPI FFH specification Committee Chair Sign Off. End date: 12/4/2023.

Technical Resources

Calendar in your own timezone

The RISC-V Technical Meetings Calendar is available in your own timezone here.

Etherpad

Etherpad, a real-time browser-based editor where users can co-edit documents instantly, is available. No login needed. Etherpad should not store permanent content. To access Etherpad, click on the here. Pads are reusable, so feel free to use the same pad for multiple meetings.
Upcoming Events

RISC-V Summit Europe 2024

RISC-V Summit Europe: June 24-28, 2024, Munich, Germany.
Glossary

- **TSC**: Technical Steering Committee
- **ARC**: Architecture Review Committee
- **IC**: ISA Committee
- **HC**: Horizontal Committee
- **SIG**: Special Interest Group
- **TG**: Task Group

Newsletter Contributions

To submit a topic for our newsletter, click here. Be sure to carefully read the submission guidelines!

Contact Information

For any queries, visit our help.riscv.org or email us at help@riscv.org.