



Technical Newsletter

2023-12-15

Volume: 7

News from TSC, ARC, ICs, HCs, SIGs and TGs

Unprivileged Spec IC

Update from the Shadow Stack and Landing Pads Task Group

The Shadow Stack and Landing Pads TG is pleased to announce the [successful completion of the architectural review](#) for the [Zlcfiss](#) extension, introducing shadow stack ISA for enhanced backward-edge control-flow integrity. The TG focus shifts towards the completion of the POC as well as the SAIL/ACT collaterals, thereby laying the groundwork for initiating the Freeze phase. We look forward to sharing further updates as our work progresses.

Security HC

Confidential Computing on RISC-V: Year-in-Review

The Trusted Computing SIG did a design survey for Confidential Computing and formed 3 focused Task Groups to develop the capabilities (ISA and non-ISA) for RISC-V platforms:

- **CoVE TG (non-ISA SW ABI):** The Confidential VM Extension (aka CoVE) TG (plan reviewed Feb'23) developed and drafted a SW ABI for scalable confidential computing for data-center (multi-tenant) server platforms leveraging the ratified H-extension and identifying ISA gaps. The TG is soliciting freeze review feedback on the specification.
- **CoVE-IO TG (non-ISA SW ABI):** This TG (recently formed Oct'23) is tasked with developing a SW ABI for device attestation and assignment for devices to be directly assigned to CoVE Confidential VMs avoiding the need for para-virtualized IO (thus avoiding buffer copies between confidential and non-confidential memory when memory is encrypted).
- **Supervisor Domains (ISA TG w/ Priv IC):** This ISA TG was co-formed (Nov'23) with the Priv IC to define the ISA extensions for supervisor domain memory isolation (Smsdid, SmMTT), interrupt assignment (Smsdia), secure external debug and IOMTT for device/IOMMU assignment to supervisor domains.

The SIG interfaced with the broader RISC-V community at the 2023 RVI Summit as well as industry consortiums such as Confidential Computing Consortium (Attestation WG) and Linux Plumbers Forum to discuss attestation formats, joint POC/upstream RFCs for related software projects (Linux-CoCo, KVM).

The Security HC is looking forward to your continued contributions to this SIG and assigned TGs as it ramps up into the freeze, public review and POC stages for the TGs.

Meeting Times

Please note the new time slots for the Security HC SIGs and assigned TGs starting January 2024. The new times are in response to BOD-requested streamlining of TG/SIG meeting times. All times are in the US Pacific time zone. Review these schedule changes and continue your active participation in the Security HC. You can find the Tech Meetings Calendar [here](#).

Odd Week Tuesdays:

- **9:00 AM:** Security Model TG (bi-weekly)
- **9:30 AM:** Runtime Integrity SIG & sPMP, IOPMP, CFI TGs, Mem. Safety, Compartmentalization (upcoming)
- **10:00 AM:** Trusted Computing SIG & Supervisor Domains (ISA) TG, CoVE and CoVE-IO (non-ISA) TGs
- **10:30 AM:** Open/HC slot

Even Week Tuesdays:

- **7:00 AM:** Trusted Computing SIG & Supervisor Domains (ISA) TG, CoVE and CoVE-IO (non-ISA) TGs
- **7:30 AM:** CHERI SIG and TG (forming)
- **8:00 AM:** Runtime Integrity SIG & sPMP, IOPMP, CFI TGs, Mem. Safety, Compartmentalization* (upcoming)
- **8:30 AM:** Security HC (bi-weekly)

SOC Infrastructure HC

Meeting Times

In line with the RVI initiative, the SoC Infrastructure HC announces new meeting schedules for its SIGs/TGs for 2024, effective January. All meetings are on Tuesdays:

- **External Debug Security TG:** Biweekly, 60 mins at 7:00 AM Pacific, starting Jan 2.
- **Server SoC TG:** Biweekly, 30 mins at 8:00 AM Pacific, starting Jan 2.

- **SoC Infra. HC:** Every 4 weeks, 30 mins at 8:30 AM Pacific, starting Jan 2.
- **Functional Safety SIG:** Biweekly, 60 mins at 9:00 AM Pacific, starting Jan 9.
- **DTPM SIG:** Every 4 weeks, 30 mins at 10:00 AM Pacific, starting Jan 9.
- **Debug TG:** Every 4 weeks, 30 mins at 10:00 AM Pacific, starting Jan 21.

These adjustments are aimed at fostering more effective and coordinated interactions within our groups, aligning with our commitment to continuous improvement in operational efficiency. Your attention to these changes and active participation in the scheduled meetings are greatly appreciated. You can find the Tech Meetings Calendar [here](#).

News from the CTO Office

Year-in-Review

Specifications

In 2023, 16 specifications were ratified:

ISA Extensions

- [Smaia, Ssaia](#) - Advanced Interrupt Architecture
- [Zacas](#) - Atomic compare-and-swap
- [Zfa](#) - Additional Scalar FP
- [Zca, Zcb, Zcd, Zce, Zcf, Zcmp, Zcmt](#) - Code Size Reduction
- [Smcntrpmf](#) - Counter Mode Filtering
- [Zicntr, Zihpm](#) - Counters
- [Zicond](#) - Conditional Ops
- [Svadu](#) - Hardware Updating of PTE A/D Bits
- [Zihintntl](#) - Non Temporal Locality Hint
- [Shcounterenw, Shvstvala, Shtvala, Shvstvecd, Shvsatpa, Shgatpa, Sscounterenw, Ssstateen, Sstvala, Sstvecd, Sstvecv, Ssu64xl, Svade, Svbare, Za128rs, Za64rs, Ziccamoa, Ziccif, Ziclsm, Ziccrse, Zic64b](#) - Profiles
- [RV32E/RV64E](#) - Reduced integer bases
- [Ztso](#) - Total Store Ordering
- [Zvbb, Zvbc, Zvkb, Zvkg, Zvkn, Zvknc, Zvkned, Zvkng, Zvknha, Zvkbnhb, Zvks, Zvksc, Zvkse, Zvksg, Zvksh, Zvkt](#) - Vector Crypto
- [Zvfh, Zvfhmin](#) - Vector IEEE FP16 Min Support, Arithmetic

NON-ISA Extensions

- [IOMMU](#) - IOMMU
- [PLIC](#) - PLIC

Technical Sessions

In 2023, we launched the RISC-V Technical Sessions, hosting a total of 11 sessions with an average of 160 registrants per session. You can review the 2023 presentations [here](#). The 2024 sessions are scheduled to begin in February 2024.

Documentation

2023 was a year of substantial achievements around RISC-V Documentation. Both the Unprivileged and Privileged Specifications conversion from LaTeX to AsciiDoc was completed. With that milestone integration of all previously ratified ISA specifications into the Unpriv and Priv specs has begun and made significant progress. Of note, the [Vector](#) and [Bitmanip](#) specifications have been converted to AsciiDoc and PR's for their integration have been issued. While review of the Vector and Bitmanip chapters takes place, conversion of the AIA and Intrinsic specs is complete, and Debug is in progress. By 1H 2024 the expectation is that all ratified specifications will exist in AsciiDoc format and all ratified ISA specifications will be fully integrated as chapters within the Unpriv or Priv specs as applicable. Following on from the integration work, presentation of a fully integrated and converted set of specifications will be released in HTML and location appropriately within the RISC-V website. Please join the [Docs SIG](#) mailing list for updates in 2024.

Development Partners

In 2023, the 5 RISC-V Development Partners of CAS/PLCT, IITM, RIOS, 10xEngineers, and Intel, along with an individual contributor (Nambi Ju), completed the following activities:

- Linux kernel support for Svnepot extension
- QEMU support for Codes Size Reduction (Zce extension)
- Priv 1.12 ACT miscellaneous test and coverage additions
- Vector SAIL support

In addition, the following items have pull requests which have been created and actively reviewed in 2023:

- LLVM and gcc support of Code Size reduction (Zce)
- PMP support in ACT
- ePMP support for SAIL and ACT
- Virtual memory support in ACT
- gcc and LLVM support for Profiles
- Zfinx and Zfh ACT support
- Vector support in Valgrind
- Basic PLIC support in SAIL
- Code Size support in SAIL
- Bitmanip and Scalar Crypto intrinsics in gcc

Additional work which was started in 2023 but has not yet reached the stage of PR submission include:

- Code Size support in ACT
- Native Trigger Debug support for ACT
- Vector support in ACT
- Priv 1.12 enhanced coverage for CSRs in ACT
- Pointer Masking SAIL and ACT
- Zdinx and Zhinx ACT
- Zvfh/Zvfhmin SAIL

In 2024, we expect to take on the following backlog items:

- Native Trigger Debug support in SAIL
- Zvfh/Zvfhmin ACT

Developer Boards

The 2023 RISC-V Developer Boards program shipped boards to various academic, distributor, labs, and individual projects of SiFive Unmatched, Xcalibyte ROMA laptops, Starfive VisionFive V2, and QWERTY Embedded Design ICE-V. Projects currently underway with Sophgo Pioneer Box, Canaan Kendryte K230, Sophgo Huashan Pi, and SiPEED Lichee Pi 4A.

If you have a project, please visit the [RISC-V Developer Boards Details page](#) and apply to the program of your choice.

Labs

In 2023, the RISC-V Labs Community completed and approved their policy [policy](#), recruited new members, supported the development of the [Cloud-V](#) lab from 10xEngineers, soft launched the program [RISC-V webpage](#), and worked toward officially naming RISC-V Lab Partners.

Notable Community Successes:

- Start of official Debian support for RISC-V as a platform [Debian support](#) using hardware hosted at multiple labs partner candidates PLCT.
- Debian CI testing on RISC-V platforms [Debian CI testing](#) hosted by PLCT
- OpenJDK CI testing on RISC-V platforms [OpenJDK CI testing](#) hosted by PLCT
- CI testing for LLaMA.cpp on RISC-V (10xEngineers)

In 2024, we look forward to refining our web presence to advertise the resources provided by partners, formally qualifying RISC-V Lab Partners who have met the criteria, and building shared documentation to help future partners.

Technical Resources

New Meeting Schedule for 2024

Starting in January 2024, the RISC-V Technical Meetings will be reorganized to better serve the community. Time slots considering the weeks of the year (2024 will have 53 weeks: 27 odd and 26 even), were allocated for the following groups:

- Privileged IC, Unprivileged IC, ISA Infrastructure HC, Profiles.
- Privileged Software HC, Applications and Tools HC, Platforms.
- SOC Infrastructure HC.
- Security HC.
- Technology HC.
- Governance (TSC, Chairs, Technical Governance).

You can see a detailed breakdown of the time slots allocated as per the approved plan [here](#).

Chairs and Vice-Chairs of SIGs and TGs are encouraged to work with their respective IC or HC in order to define the best time slot for their meetings. ICs and HCs Chairs and Vice-Chairs are also encouraged to work with their peers in order to accommodate all meetings in the best possible way.

Action Required for Chairs and Vice-Chairs: LFX and RISC-V Jira Account Creation

Please, read the following instructions carefully only if you are not able to access RISC-V Jira or has never accessed it before.

We are moving to Jira. In order to access RISC-V Jira, it is required to have a LFX account. If you do not have a LFX account, please create one by clicking [here](#).

Once you have created your LFX account, please login in RISC-V Jira by clicking [here](#).

In order to access the resources within RISC-V Jira, you will need to be added to the right group. Please open an issue at help.riscv.org and provide the following information: LFX email address and Jira username. We will add you to the right group and you will receive an email notification once you have been added.

If you **cannot** access help.riscv.org, please send an email to help@riscv.org with your GitHub ID so we can add you to the help repository.

Calendar in your own timezone

The **RISC-V Technical Meetings Calendar** is available in your own timezone [here](#).

Etherpad

Etherpad, a real-time browser-based editor where users can co-edit documents instantly, is available. No login needed. Etherpad should not store permanent content. To access Etherpad, click on the [here](#). Pads are reusable, so feel free to use the same pad for multiple meetings.

News from the Community

An open-source RISC-V Input/Output Memory Management Unit (IOMMU)

A team led by Sandro Pinto, founder of Zero-Day Labs and professor at the University of Minho, and supported by RISC-V International's strategic member, TII's Secure Systems Research Center, has released the first open-source RISC-V Input/Output Memory Management Unit (IOMMU). This IOMMU is compliant with the ratified v1.0 [specification](#). The IIP is highly parameterizable and supports all mandatory and optional features, except for PCI-related [functionalities](#). The IOMMU has been integrated into a RISC-V SoC alongside the CVA6 CPU, and it has been functionally validated with Linux and the Bao [hypervisor](#). Preliminary plans are underway to start IP verification as a joint venture between Zero-Day Labs and 10xEngineers. Manuel Rodriguez, the principal architect and developer of the IOMMU, is encouraging contributions from external parties. The aim is to establish this IP as the reference open-source IOMMU for the RISC-V ecosystem.

Upcoming Events

RISC-V Summit Europe 2024

[RISC-V Summit Europe](#): June 24-28, 2024, Munich, Germany.

Glossary

- **TSC:** Technical Steering Committee
- **ARC:** Architectural Review Committee
- **IC:** ISA Committee
- **HC:** Horizontal Committee
- **SIG:** Special Interest Group
- **TG:** Task Group

Newsletter Contributions

To submit a topic for our newsletter, [click here](#). Be sure to carefully read the submission guidelines!

Contact Information

For any queries, visit our help.riscv.org or email us at help@riscv.org.

