



Technical Newsletter

2024-01-30

Volume:

News from TSC, ARC, ICs, HCs, SIGs and TGs

Architecture Review Committee (ARC)

Meeting Minutes

The ARC met on 2024-01-09 and the highlights of the meeting are the following:

- ARC grants official AR approval for the [Pointer-Masking](#) and [RERI](#) extensions.
- New pointer masking options (Supm, Sspm) have to be added to the RVA23/RVB23 profiles.
- Sstrict is to be described and added as an option to the RVA profiles.
- Zicclsm (Main memory supports misaligned loads/stores) spec does mandate vector misaligned support, and that this is the correct thing to do.

The complete meeting minutes can be found [here](#).

Unprivileged Spec IC

Attached and Integrated Matrix Task Groups

The initial two task groups that spun out of the Vector SIG have defined their meetings times:

- Attached Matrix TG: Every odd week on Monday at 7:00 am Pacific.
- Integrated Matrix TG: Every odd week on Monday (alternate with SIG Vector) at 8:00 am Pacific.

Both meeting schedules and their Zoom credentials can be found at tech.riscv.org/calendar/.

Pointer Masking is Getting Ready for Public Review

The pointer masking standard has passed architecture review and is preparing for public review. The latest draft spec is [here](#). If you are an implementer, or are interested in software support for pointer masking, this is a good time to give the standard another look.

Security HC

High Assurance Cryptography

The Security HC, on behalf of the Unprivileged ISA Committee are pleased to announce the approval of the [High Assurance Cryptography Task Group](#).

The current charter of the High Assurance Cryptography TG can be found [here](#) and the mailing list [here](#).

SOC Infrastructure HC

Enhanced Trace for RISC-V

Revision 2.0.1 of the Enhanced Trace for RISC-V (E-Trace) Specification [has been published](#). The primary change is to remove the control field definitions and reference instead the RISC-V Trace Control Interface Specification. There are also a number of non-normative corrections and clarifications.

ISA Infrastructure HC

New Meeting Time for Sail Golden Model

Starting with the new year, the weekly meeting of the tech-golden-model meeting (the RISC-V Sail model), has been moved to Mondays at 07:00 am (US Pacific), 3:00 pm (UK and most of Europe), 11 pm (China).

During the meeting, the TG focus on prioritizing Pull Requests (PRs) and addressing outstanding issues. Additionally, they dedicate time to discussing a range of technical concerns related to the model, ensuring a comprehensive approach to its development and refinement.

Questions? Contact Bill McSpadden at bill@riscv.org.

News from the CTO Office

IMPORTANT

Groups.io Revalidation

Some members have been sent an email with the subject Action Required: Confirm Your Groups.io Membership to Continue Receiving Group Emails. It asks the member to either respond to the email or log into their account in order to confirm their membership. Most such accounts are ones that haven't posted in a long time. It's important that all know that this email is legit. It's not a phish.

If you got this and didn't revalidated the access, probably your Groups.io account has been suspended. Please contact help@riscv.org if needed so we can help you to revalidate your account.

A full description of this revalidation can be found [here](#).

Recently Approved Fast-Track Plans

- [Zba,Zbb,Zbs. B.](#)
- [Svvptc. No Caching of Invalid PTEs.](#)
- [Zaamo,Zalrsc. A Extension Components.](#)

Public Review

- [May-Be-Operations](#). End date: **2024-02-09**. The link to the announcement can be found [here](#).
- [Supervisor Counter Delegation](#). End date: **2024-02-17**. The link to the announcement can be found [here](#).
- [Debug for Hardware Platforms](#). End date: **2024-02-18**. The link to the announcement can be found [here](#).

Call for Candidates

- **Call for Chair/Vice-chair Candidates for the Server Platform TG**. The call is open until **January 30, 2024** and can be found [here](#).
- **Call for Chair/Vice-chair Candidates for the Profiles SIG**. The call is open until **January 31, 2024** and can be found [here](#).
- **Call for Chair/Vice-chair Candidates for the Platform Management Interface (RPMI) TG**. The call is open until **February 12, 2024** and can be found [here](#).

If you want to nominate yourself or someone else for any of the open positions, please email help@riscv.org.

Votes

TSC

- The Fast Track Extension [Indirect Control and Status Register \(CSR\) Access](#) was approved to be sent to the Board of Directors for Ratification (Feb 29, 24). Vote ended on 2024-01-26. The results can be found [here](#).

HC & IC Committees

- [Quality-of-Service \(QoS\) Identifiers](#) and [Capacity and Bandwidth controller QoS Register Interface \(CBQRI\)](#) are Frozen. They now move to the Ratification-Ready phase and the public review should start shortly.
- Freeze Milestone for [Byte and Halfword Atomic Memory Operations](#) Fast Track Ext Committee Chair Sign Off. Vote ends on **2024-01-31**. The vote status can be found [here](#).
- Freeze Milestone for [RAS Error Record Interface \(RERI\)](#) Non-ISA Spec Committee Chair Sign Off. Vote ends on **2024-02-09**. The vote status can be found [here](#).

Technical Resources

Active ICs, HCs, SIGs and TGs

You can find the list of active ICs, HCs, SIGs and TGs at tech.riscv.org/groups. If you find any inconsistencies, please report it via help@riscv.org or help.riscv.org. A similar page for all Extensions is under development.

Jira@RISC-V

As we continue to grow, we are working to improve our tools and processes to better serve the community. We are moving to Jira to manage the specification development process and groups lifecycle. The Jira@RISC-V instance is available at jira.riscv.org. We are currently in the process of migrating the existing issues to Jira but would like to invite you to access it using your [Linux Foundation account](#). No other action is required at this time.

Tools Access

You can verify your access the current set of tools used within RISC-V International at tech.riscv.org. If you find any inconsistencies, please contact help@riscv.org.

Technical Meetings Calendar Adjusted to Your Local Time Zone

The **RISC-V Technical Meetings Calendar** is available in your own timezone [here](#).

Tech Preview: One-stop-shop for RISC-V Technical Meetings

The RVI Technical Staff is consolidating all key information for meetings in a single place. The [RISC-V Technical Meetings](#) page is a one-stop-shop for all RISC-V technical meetings. It includes guidelines, tutorials, and more. The page is still under development, so please send us your feedback via help@riscv.org.

Etherpad

Etherpad, a real-time browser-based editor where users can co-edit documents instantly, is available. No login needed. Etherpad should not store permanent content. To access Etherpad, click on the [here](#). Pads are reusable, so feel free to use the same pad for multiple meetings.

Technical Sessions

The 2024 season of the RISC-V Technical Sessions starts on February 1st, 7 am Pacific Time. The presentation is titled **InspireSemi Thunderbird Compute Accelerator Overview** and will be presented by **InspireSemi**. You can find more information and register [here](#).

Upcoming Events

- [Open Source Summit North America](#): April 16-18, 2024, Seattle, Washington.
- [RISC-V Summit Europe](#): June 24-28, 2024, Munich, Germany.

Glossary

- **TSC:** Technical Steering Committee
- **ARC:** Architectural Review Committee
- **IC:** ISA Committee
- **HC:** Horizontal Committee
- **SIG:** Special Interest Group
- **TG:** Task Group

Newsletter Contributions

To submit a topic for the Technical Newsletter, [click here](#). Be sure to carefully read the submission guidelines!

Contact Information

For any queries, visit help.riscv.org or email us at help@riscv.org.

