News from TSC, ARC, ICs, HCs, SIGs and TGs

Privileged Spec IC

Internal Review of the Privileged Architecture Specification v1.13

The Privileged Architecture ISA Committee has released a draft of the Privileged Architecture spec version 1.13, featuring minor clarifications and improvements over 1.12, detailed in the preface. For an internal review, submit feedback through GitHub issues with the "Privileged Architecture v1.13" label or discuss broader issues on the mailing list.

Privileged Software HC

Boot and Runtime Services (BRS)

The Boot and Runtime Services (BRS) TG invites reviews of the draft BRS specification, now ready for wider feedback. Access the spec here. You can provide feedback via GitHub issues or the mailing list.

Security HC

RISC-V Confidential VM Extension (CoVE) ABI Specification: Internal Review Completed

The internal review of the RISC-V Confidential VM Extension (CoVE) ABI specification, a key deliverable from the AP-TEE TG under the Security HC, has successfully concluded. All comments and feedback have been documented as GitHub issues and a stable version of the CoVE specification will be made available on the GitHub repository following the completion of these updates.

SOC Infrastructure HC

Internal Review of the Server SoC Specification

The Server SoC specification TG invites community feedback on the RISC-V Server SoC Specification, aiming to standardize capabilities for system software. Access the spec here and provide feedback via the mailing list or by opening GitHub issues by March 1.

ISA Infrastructure HC

Documentation

Integration of New Extensions as Part of the Privileged Spec

The integration process will unfold in two distinct phases.

- **Initial PR Submission**: The first phase involves the submission of a Pull Request (PR) that incorporates the existing specification as a new chapter without altering any other part of the document. This step allows us to maintain the integrity of the current spec while beginning the integration of new content.

- **Secondary PR for Full Integration**: Following the initial PR's merger, a second PR will be submitted. This PR aims for the comprehensive integration of the specification, with contributions from the original authors and other relevant stakeholders to ensure a seamless merge into the existing document.

PRs from the first phase can be merged at any time, given their non-intrusive nature. PRs from the second phase require thorough review and approval by the ISA Committee chairs. These PRs must not only be semantically accurate but consistent with the current spec style and aesthetic criteria.

News from the CTO Office

Call for Candidates

As of today, February 16, 2024, the following groups have submitted a call for candidates:

SIGs

- Documentation
- Debug, Trace and Performance Monitoring
- Functional Safety
- HPC
- Microarchitectural Side Channels
- Performance Analysis
- Performance Modeling
- Runtime Integrity
- SoftCPU
- Trusted Computing

TGs

- CoVE (AP-TEE)
- Control Transfer Records (CTR)
- IOPMP
- Platform Runtime Services (PRS)
- Shadow Stack and Landing Pads

Target Dates

Here are the target dates for the election process:

- All calls must have commenced by Friday, February 23rd.
- Closure of Calls: Friday, March 8th.
- Completion of Voting/Selections: Friday, March 29th.

How to Submit a Call for Candidates

The Chair/Vice-Chair of a group can submit a "Call for Candidates" by following these steps:

- Visit help.riscv.org (a GitHub login is required).
- Create a New Call for Candidates issue.

  Upon creation, a draft email template will automatically be generated within the issue. You can modify this template to suit your specific requirements. Here is an example for reference.

- After finalizing the "Call for Candidates" email, distribute it to the following mailing lists:

  tech-announce@lists.riscv.org

  The governing IC/HC mailing list (you can find it here)

  All dotted-lined committees (you can find it here)

  The specific group mailing list (you can find it here)

- As the RISC-V staff begins to receive applications, they will move forward with the subsequent steps in the process.

Nomination Process

If you want to nominate yourself or someone else, please email **help@riscv.org**.

Recently Approved Fast-Track Plans

- **Zalasr**: Load-Acquire/Store-Release. The Fast-Track Plan was approved on Wed, Feb 14, 2024. The extension is now officially under development. The next step, once the development is complete, is to conduct an Internal Review.

Public Review

In Progress

- Supervisor Counter Delegation. End date: **2024-02-17**. The link to the announcement can be found here.
- Debug for Hardware Platforms. End date: **2024-02-18**. The link to the announcement can be found here.

Completed

- May-Be-Ops. The summary of the public review can be found here.

Votes

TSC

- **Approve the Platform Management Interface (RPMI) Task Group**. End date: **2024-02-29**. The link to the text of the voting can be found here. The OpaVote can be found here.

HC & IC Committees

- **Freeze Milestone for Resumable Non-Maskable Interrupts Fast Track Extension**. Jira. End date: **2024-02-19**. The link to the text of the voting can be found here. The OpaVote can be found here.

- **Freeze Milestone for A Extension Components (Zaamo and Zalrsc) Fast Track Extensions**. Jira. End date: **2024-02-19**. The link to the text of the voting can be found here. The OpaVote can be found here.

- **Freeze Milestone for B Extension Components (Zba, Zbb, Zbs) Fast Track Extension**. Jira. End date: **2024-02-19**. The link to the text of the voting can be found here. The OpaVote can be found here.

- **Freeze Milestone for RAS Error Record Register Interface NON-ISA Extension**. Jira. End date: **2024-02-09** (Still Open). The link to the text of the voting can be found here. The OpaVote can be found here.

- **Freeze Milestone for Pointer Masking Extension**. Jira. End date: **2024-01-29** (Still Open). The link to the text of the voting can be found here. The OpaVote can be found here.

- **Freeze Milestone for QoS Ids Fast Track and the CBQRI NON-ISA Extension**. QoS Jira and CBQRI Jira. End date: **2024-01-26** (Still Open). The link to the text of the voting can be found here. The OpaVote can be found here.

Technical Resources

RISC-V Software Ecosystem Dashboard

The RISC-V Software Ecosystem Dashboard is a new tool that provides a comprehensive view of the RISC-V software ecosystem. It includes information on the status of RISC-V in software projects, tools, and libraries. The dashboard is under development and available at here.

You can contribute to the RISC-V Software Ecosystem by visiting https://tech.riscv.org/ecosystem-contribution.

Active ICs, HCs, SIGs and TGs

You can find the list of active ICs, HCs, SIGs and TGs at tech.riscv.org/groups. If you find any inconsistencies, please report it via help@riscv.org or help.riscv.org. A similar page for all Extensions is under development.

Jira@RISC-V

We are moving to Jira to manage the specification development process and groups lifecycle. The Jira@RISC-V instance is available at jira.riscv.org. We are currently in the process of migrating the existing issues to Jira but would like to invite you to access it using your Linux Foundation account. No other action is required at this time.

Technical Meetings Calendar Adjusted to Your Local Time Zone

The **RISC-V Technical Meetings Calendar** is available in your own timezone here.

One-stop-shop for RISC-V Technical Meetings

The RVI Technical Staff is consolidating all key information for meetings in a single place. The RISC-V Technical Meetings page is a one-stop-shop for all RISC-V technical meetings. It includes guidelines, tutorials, and more. The page is still under development, so please send us your feedback via help@riscv.org.

Etherpad

Etherpad, a real-time browser-based editor where users can co-edit documents instantly, is available. No login needed. Etherpad should not store permanent content. To access Etherpad, click on the here. Pads are reusable, so feel free to use the same pad for multiple meetings.

Technical Sessions

InspireSemi Thunderbird Compute Accelerator Overview

The recording of the latest RISC-V Technical Session, "InspireSemi Thunderbird Compute Accelerator Overview," is now available on the RISC-V YouTube channel.

Upcoming Events

- Open Source Summit North America: April 16-18, 2024, Seattle, Washington.
- RISC-V Summit Europe: June 24-28, 2024, Munich, Germany.

Glossary

- **TSC**: Technical Steering Committee
- **ARC**: Architectural Review Committee
- **IC**: ISA Committee
- **HC**: Horizontal Committee
- **SIG**: Special Interest Group
- **TG**: Task Group

Newsletter Contributions

To submit a topic for the Technical Newsletter, click here. Be sure to carefully read the submission guidelines!

Contact Information

For any queries, visit help.riscv.org or email us at help@riscv.org.

riscv.org