



Technical Newsletter

2024-03-30

Volume: 13

News from TSC, ARC, ICs, HCs, SIGs and TGs

Technical Steering Committee (TSC)

Fast-Track for NON-ISA Specifications

Many have been under the impression — a notion more akin to rumor than fact — that Fast-Tracks are exclusive to ISA developments. However, the [Fast-Track policy](#) accommodates both ISA and Non-ISA Fast-Tracks!

The necessary documentation will be updated to clarify this.

Profiles & Platforms

The Profiles SIG completed the election process and the new Chair and Vice-Chair are **David Weaver (Akeana)** and **James Ball (Qualcomm)**, respectively. The link to the announcement can be found [here](#).

Here are the details about the new SIG:

- **Chair:** David Weaver (Akeana)
- **Vice-Chair:** James Ball (Qualcomm)
- **Mailing List:** <https://lists.riscv.org/g/sig-profiles>
- **Jira:** <https://jira.riscv.org/browse/RVG-156>
- **Meetings:** The first meeting is planned for Thu 18 Apr at 9am Pacific Time. Bookmark the [RISC-V Tech Meetings](#) and do not miss this one.

Architecture Review Committee (ARC)

Meeting Minutes

The latest ARC meeting minutes is available can be found in the link below:

- 2024-03-19: <https://lists.riscv.org/g/tech-unprivileged/message/744>

Unprivileged Spec IC

Internal Review for Zalasr (Load-Acquire Store-Release) Extension

The Internal Review Period for Zalasr is open. You can find the announcement [here](#). The Zalasr extension adds load-acquire and store-release instructions in byte through doubleword sizes, allowing for more efficient atomic code and closing a gap in the psABI.

Technology HC

New Chair and Vice-Chair for HPC SIG

The Special Interest Group for High Performance Computing ([Jira](#)) has elected a new chair and vice-chair. Dr. Nick Brown (EPCC, the University of Edinburgh) and Dr. Teresa Cervero (Barcelona Supercomputing Center) will serve as the new Chair and Vice-Chair, respectively. The announcement can be found [here](#).

ISA Infrastructure HC

Documentation

After a considerable effort, all Ratified specifications up to and including March 2024 have been integrated into the Unprivileged and Privileged specifications. The prefaces and change logs for each specification are in the final stage of being updated, and PDFs of both specs will be distributed for internal review as soon as that's complete.

The following extensions have been included in this document since the last published RISC-V ISA specifications in 2019 (Unpriv) and 2021 (Priv):

- **RV32E/RV64E** - Base integer instruction sets
- **Sm1p12, Ss1p12, Sv57, Hypervisor, Svinval, Svnapot, Svpbmt** - Priv 1.12, and virtual memory extensions
- **Smcntrpmf** - Cycle and instret privilege mode filtering
- **Smempmp** - PMP enhancements for memory access and execution prevention in machine mode
- **Smstateen** - State enable extension
- **Sscofpmf** - Count overflow and mode-based filtering extension
- **Sstc** - Time compare
- **Svadu** - Hardware updating of PTE A/D bits

- **Zacas** - Atomic compare-and-swap instructions
- **Zawrs** - Wait-on-Reservation-Set extension
- **Zba, Zbb, Zbc, Zbs** - Bit-manipulation extensions
- **Zbkb, Zbkc, Zbkx, Zknd, Zkne, Zknh, Zksed, Zksh, Zkn, Zks, Zkt, Zk, Zkr** - Cryptography extensions Volume 1 (scalar)
- **Zca, Zcb, Zcd, Zce, Zcf, Zcmp, Zcmt** - Code size reduction extensions
- **Zfa** - Standard extension for additional floating-point instructions
- **Zfh, Zfhmin** - Standard extensions for half-precision floating-point
- **Zfinx, Zdinx, Zhinx, Zhinxmin** - Standard extensions for floating-point in integer registers
- **Zicbom, Zicbop, Zicboz** - Cache management operation extensions
- **Zicntr, Zihpm** - Counters
- **Zicond** - Integer conditional operations extension
- **Zihintntl** - Non-temporal locality hints
- **Zihintpause** - Pause hint
- **Zmcsrind, Sscsrind** - Indirect CSR access extensions
- **Zmmul** - Multiplication subset of the M extension
- **Ztso** - Total Store Ordering extension
- **Zvbb, Zvbc, Zvkb, Zvkg, Zvkn, Zvknc, Zvkned, Zvkng, Zvknha, Zvknhb, Zvks, Zvksc, Zvksed, Zvksg, Zvksh, Zvkt** - Cryptography extensions Volume 2 (vector)
- **Zve32x, Zve32f, Zve64x, Zve64f, Zve64d, Zve, Zvl32b, Zvl64b, Zvl128b, Zvl256b, Zvl512b, Zvl1024b, Zvl, Zv** - Vector extension
- **Zvfh, Zvfhmin** - Half-precision floating-point vector arithmetic (full and minimal)

The implications of integration is that all issues with any of these specifications will be logged against the [riscv-isa-manual](#) repository for consideration. Original development repositories have been or will be archived for reference and any outstanding issues transferred to the [riscv-isa-manual](#) repository.

In addition, the specification lifecycle has been updated for ISA specifications to include freeze requirement steps to issue a Pull Request against the [riscv-isa-manual](#) for integration of new specifications going forward.

All future issues with these extensions should be filed against the [riscv-isa-manual](#) GitHub repository.

News from the CTO Office

Groups

Call for Candidates

The following are the open calls for Chair/Vice-Chair candidates:

SIGs

- [AI/ML](#)
- [Architectural Compatibility Test](#)

Nominations

If you want to nominate yourself or someone else, please email help@riscv.org.

Extensions

Under Public Review

- [Quality-of-Service \(QoS\) Identifiers](#) and [Capacity and Bandwidth controller QoS Register Interface \(CBQRI\)](#). End date: **2024-04-05**. The link to the announcement can be found [here](#).
- [Pointer Masking \(J\)](#). End date **Apr 19, 2024**. The link to the announcement can be found [here](#).
- [Resumable Non-maskable Interrupts](#). End date **Apr 19, 2024**. The link to the announcement can be found [here](#).
- [Shadow Stacks and Landing Pads](#). End date **Apr 27, 2024**. The link to the announcement can be found [here](#).

Public Review Recently Completed

- [B Extension Components](#). End date: **2024-03-22**. The link to the announcement can be found [here](#).
- [A Extension Components](#). End date: **2024-03-27**. The link to the announcement can be found [here](#).
- [RAS Error Record Interface \(RERI\)](#). End date: **2024-03-29**. The link to the announcement can be found [here](#).

Recently Ratified

- **2024-03-28.** May-Be-Operations version 1.0 (Zimop, Zcmop) ([PDF](#), [Jira](#)) led by **Andrew Waterman** and **Ved Shanbhogue** under the governance of the Unprivileged ISA Committee.
- **2024-03-28.** Supervisor Counter Delegation version 1.0 (Smcdeleg, Ssccfg) ([PDF](#), [Jira](#)) led by **Beeman Strong** under the governance of the Privileged ISA Committee.

Votes

HC & IC Committees

- **Ratification-Ready Milestone for B Extension.** [Jira](#). End date: **2024-04-02**. The link to the text of the voting can be found [here](#). The OpaVote can be found [here](#).
- **Freeze Milestone for E-Trace Encapsulation.** [Jira](#). End date: **2024-04-03**. The link to the text of the voting can be found [here](#). The OpaVote can be found [here](#).

Technical Resources

Active ICs, HCs, SIGs and TGs

You can find the list of active ICs, HCs, SIGs and TGs at tech.riscv.org/groups.

Extensions Under Development

The status of extensions under development is available at tech.riscv.org/extensions.

Software Ecosystem Dashboard

The Software Ecosystem Dashboard is available at tech.riscv.org/software-ecosystem.

Technical Meetings Calendar Adjusted to Your Local Time Zone

The **RISC-V Technical Meetings Calendar** is available in your own timezone [here](#).

One-stop-shop for Technical Resources

The tech.riscv.org page is a one-stop-shop for all RISC-V technical content. Bookmark it!

Etherpad

Etherpad, a real-time browser-based editor where users can co-edit documents instantly, is available. No login needed. Etherpad should not store permanent content. To access Etherpad, click on the [here](#). Pads are reusable, so feel free to use the same pad for multiple meetings.

Technical Sessions

Recording

The latest RISC-V Technical Session entitled **A Framework for RISC-V SBI and ISA Extension Validation**, which was presented by Andrew Jones, Principal Software Engineer at Ventana Micro Systems, is now available on YouTube. [Watch it here!](#)

Tech Sessions on YouTube

We are uploading all Technical Sessions to the RISC-V YouTube channel. You can find the playlists for the 2023 Sessions [here](#). The 2024 Sessions are available [here](#).

Upcoming Events

- [Embedded World](#) April 9-11, 2024, Nuremberg, Germany.
- [Open Source Summit North America](#): April 16-18, 2024, Seattle, Washington.
- [RISC-V Summit Europe](#): June 24-28, 2024, Munich, Germany.
- [Hot Chips 2024](#). The Hot Chips 2024 Call for Presentations info just went live on the Hot Chips web site.

The event will be held as a hybrid conference with in-person attendance at Memorial Auditorium, Stanford University from August 25 to 27, 2024.

The submission deadline was extended to April 10, 2024.

Note that **having silicon** is not a requirement for a Hot Chips presentation. In fact, presentations about IP products, cooling technology, software tools, etc, etc are welcome (see suggested topic list, which is not meant to be exhaustive, on the web page). Any topic that “sounds interesting & relevant to the Program Committee” can be accepted.

Please contact Dave Weaver (david.weaver@akeana.com) for more information.

Glossary

- **TSC:** Technical Steering Committee
- **ARC:** Architectural Review Committee
- **IC:** ISA Committee
- **HC:** Horizontal Committee
- **SIG:** Special Interest Group
- **TG:** Task Group

Newsletter Contributions

To submit a topic for the Technical Newsletter, [click here](#). Be sure to carefully read the submission guidelines!

Contact Information

For any queries, visit help.riscv.org or email us at help@riscv.org.

