News from TSC, ARC, ICs, HCs, SIGs and TGs

Architecture Review Committee (ARC)

Meeting Minutes

The latest ARC meeting minutes is available can be found in the link below:

- 2024-04-24: https://lists.riscv.org/g/tech-privileged/message/1910

ISA Infrastructure HC

SAIL

There is a lot of activity in the RISC-V Sail model. Here are some of the recent changes:

- On March 26, Carl Friedrich Bolz-Tereick gave a presentation to the Golden Model ISG (linkhttps://lists.riscv.org/g/tech-golden-model[tech-golden-model]) about his work in using JIT techniques to improve the performance of models written in Sail, including the RISC-V formal model. You can watch the recording of the presentation here. The slides are available here.

- Rishiyur Nikhil (Bluespec) refactored the VM code in the RISC-V Sail model in order improve maintenance of the VM, a classic instance of anti-programming. For years, the RISC-V Sail model had lived with 3 blocks of code that implemented SV32, SV39 and SV48 Virtual Memory. These blocks of code were largely the same. Nikhil recognized that the Sail language should allow the ability to parameterize a common set of code that could be instantiated to implement any of the Virtual Memory models. See PR #408 for more information.

- The compilation process for the RISC-V Sail model inadvertently missed an incorrect vector length specification when building fro 32-bit floating point. Tim Hutt (Codasip) fixed this issue. See PR #441 for more information.

- The RISC-V Unrpiv spec describes the compressed instructions C.SRAI and C.SRLI and puts restrictions on the shamt[5] field. The restriction check was missing on the C.SRAI and C.SRLI but was present for the C.SLLI instruction. Tim Hutt (Codasip) fixed this issue. See PR #440 for more

information.

- [Tim Hutt (Codasip)](#) found an issue with the encoding of Medeleg register related to the MEnvCall event: the wrong bit was designated for the event (bit 10 instead of bit 11). See [PR #438](#) for more information.

- Change to standard nomenclature: 'atom' replaced with 'int'. The Sail language prefers the usage of type 'int' rather than type 'atom'. PR #437 replaces all instances of 'atom' with 'int'. See [PR #437](#) for more information.

- [Alasdair Armstrong (Cambridge)](#) found a typo in the string that is associated with the E_SAMO_Addr_Align exception. See [PR #431](#) for more information.

- Cleanup of compiler warnings: PRIu64 for printing uint64_t. The compilation of the RISC-V model had several warnings that needed to be cleaned up. These related to printing out 64-bit values. [Tim Hutt (Codasip)](#) fixed this issue. See [PR #417](#) for more information.

- Fix senvcfg CSR definition. The senvcfg implementation was improperly treated the same as menvcfg. [Ved Shanbhogue (Rivos)](#) added separate implementations (and legalization functions) for menvcfg and senvcfg. See [PR #413](#) for more information.

- Added m/senvcfg to CSR name map. In the model's CSR map, the senvcfg and menvcfg CSRs did not exist. [Tim Hutt (Codasip)](#) added these CSRs to the map. See [PR #405](#) for more information.

- Code cleanup around PMP implementation. There is is ongoing work being done to better support CBOs and PMAs. [Tim Hutt (Codasip)](#) has cleaned up some of the code around memory checking to better support these features (and to make the code more readable). See [PR #435](#) for more information.

Documentation

Doc SIG is Getting Started

The Doc SIG is forming! Until the meeting time is set and our charter is updated, you can join in discussions in the Doc SIG [mailing list](#) and in the [Doc requirements GitHub repo](#).

Initial Draft of the Integrated ISA Specification | Action Required!

All Members are invited to review the initial draft of the integrated ISA specification, which includes Volumes I and II covering all ratified content to date. Please provide feedback on the format and layout, and help identify any errors from the transliteration process. This review does not introduce new ISA features but aims to refine the presentation of existing extensions.

- **Review Period:** April 12, 2024 - April 26, 2024

- **Access the Drafts:** [Volume I: Unprivileged](#) | [Volume II: Privileged](#)

- **Source Repository:** GitHub - [RISC-V Instruction Set Manual](#)

Feedback Submission:

- **Email:** isa-dev@lists.riscv.org

- **GitHub:** Issues or PRs

Corrections and suggestions will be reviewed by the ISA Committees and the Documentation Team. Minor and non-controversial changes will be directly incorporated, with other revisions planned for future updates.

News from the CTO Office

RISC-V Software Ecosystem

Over the past month, there has been a 29% increase in the number of software projects we track. Currently, we are listing 89 projects along with their RISC-V support statuses. You can view these details on our dashboard at tech.riscv.org/software-ecosystem.

Groups

RISC-V Task Group and Special Interest Group Selections for 1Q 2024

The initial results for the RISC-V Task Group (TG) and Special Interest Group (SIG) selections for the first quarter have been announced. These positions will be held for a one-year term starting from April 1, 2024.

Group Name	Chair	Vice-chair	Type
Android	Han Mao (Alibaba)	Elliott Hughes (Google)	SIG
Architecture Test	James Shi (Alibaba)	Umer Shahid (10X Engineers)	SIG
Debug, Trace, and Performance Monitoring (DTPM)	Iain Robertson (Siemens)	Paul Donahue (Ventana Micro Systems)	SIG
Documentation	Kevin Broch (Rivos Inc.)	-	SIG
Functional Safety	Daniel Gracia (Thales Group)	-	SIG
Microarchitecture Side Channels	Ronan Lashermes (Inria)	Allison Randal (Individual)	SIG
Performance Analysis	Beeman Strong (Rivos Inc.)	-	SIG
Performance Modeling	Arup Chakraborty (Ventana Micro Systems)	Knute Lingaard (MIPS)	SIG
Runtime Integrity	Nick Kossifidis (Forth)	Deepak Gupta (Rivos Inc.)	SIG

Group Name	Chair	Vice-chair	Type
Soft CPU	Guy Lemieux (Individual)	Jan Gray (FPGA)	SIG
Trusted Computing	Ravi Sahita (Rivos Inc.)	-	SIG
AP-TEE (CoVE)	Ravi Sahita (Rivos Inc.)	Guerney Hunt (IBM)	TG
Control Transfer Records	Beeman Strong (Rivos Inc.)	Bruce Ableidinger (SiFive)	TG
Fast Interrupts (CLIC)	Dan Smathers (Seagate)	Jean-Baptiste Brelot (Nordic Semi)	TG
I/O Physical Memory Protection Unit (IOPMP)	Paul Ku (Andes)	Channing Tang (NVIDIA)	TG
Pointer Masking (J)	Martin Maas (Google)	-	TG
Nexus	Robert Chyla (MIPS)	Jay Gamoneda (NXP)	TG
Platform Runtime Services	Atish Patra (Rivos Inc.)	Sunil VL (Venta Micro Systems)	TG
S-Mode Physical Memory Protection (SPMP)	Dong Du (Shanghai Jiao Tong University)	-	TG
Security Model	Paul Elliot (Codasip)	-	TG
Shadow Stack & Landing Pads	Giorgos Christou (Technical University of Crete)	Ved Shanbhogue (Rivos Inc.)	TG

Open Call for Candidates

The following are the open calls for Chair/Vice-Chair candidates:

SIGs

- AI/ML

- Architectural Compatibility Test

- QEMU

TGs

- Performance Events

Nominations

If you want to nominate yourself or someone else, please email **help@riscv.org**.

Extensions

Under Public Review

- Pointer Masking (J). End date **Apr 19, 2024**. The link to the announcement can be found here.

- Resumable Non-maskable Interrupts. End date **Apr 19, 2024**. The link to the announcement can be found here.

- Shadow Stacks and Landing Pads. End date **Apr 27, 2024**. The link to the announcement can be found here.

- E-Trace Encapsulation. End date **May 10, 2024**. The link to the announcement can be found here.

Public Review Recently Completed

- Quality-of-Service (QoS) Identifiers and Capacity and Bandwidth controller QoS Register Interface (CBQRI). End date: **2024-04-05**. The link to the announcement can be found here.

Active Votes

TSC

- **Send B Extension Components (Zba, Zbb, Zbs) to the Board for Ratification**. Jira. End date: **2024-04-19**. The link to the text of the voting can be found here. The OpaVote can be found here.

- **Approve the Server Platform Task Group**. Jira. End date: **2024-04-22**. The link to the text of the voting can be found here. The OpaVote can be found here.

- **Send A Extension Components (Zaamo, Zalrsc) to the Board for Ratification**. Jira. End date: **2024-04-24**. The link to the text of the voting can be found here. The OpaVote can be found here.

HC & IC Committees

- **Ratification-Ready Milestone for Eliding Memory-Management Fences on Setting PTE Valid**. Jira. End date: **2024-04-17**. The link to the text of the voting can be found here. The OpaVote can be found here.

- **Ratification-Ready Milestone for RAS Error Record Interface (RERI)**. Jira. End date: **2024-04-17**. The link to the text of the voting can be found here. The OpaVote can be found here.

Technical Resources

One-stop-shop for Technical Resources

The tech.riscv.org page is your one-stop-shop for all RISC-V technical content. Bookmark it!

Active ICs, HCs, SIGs and TGs

You can find the list of active ICs, HCs, SIGs and TGs at tech.riscv.org/groups.

Extensions Under Developmment

The status of extensions under development is available at tech.riscv.org/extensions.

Software Ecosystem Dashboard

The Software Ecosystem Dashboard is available at tech.riscv.org/software-ecosystem.

Technical Meetings Calendar Adjusted to Your Local Time Zone

The **RISC-V Technical Meetings Calendar** is available in your own timezone here.

Etherpad

Etherpad, a real-time browser-based editor where users can co-edit documents instantly, is available. No login needed. Etherpad should not store permanent content. To access Etherpad, click on the here. Pads are reusable, so feel free to use the same pad for multiple meetings.

Tech Sessions on YouTube

We are uploading all Technical Sessions to the RISC-V YouTube channel. You can find the playlists for the 2023 Sessions here. The 2024 Sessions are available here.

Upcoming Events

- Open Source Summit North America: April 16-18, 2024, Seattle, Washington, USA.

- RISC-V Summit Europe: June 24-28, 2024, Munich, Germany.

- Hot Chips 2024. August 25-27, 2024. Memorial Auditorium, Stanford University, Stanford, California, USA.

Glossary

- **TSC**: Technical Steering Committee
- **ARC**: Architectural Review Committee
- **IC**: ISA Committee
- **HC**: Horizontal Committee
- **SIG**: Special Interest Group
- **TG**: Task Group

Newsletter Contributions

To submit a topic for the Technical Newsletter, click here. Be sure to carefully read the submission guidelines!

Contact Information

For any queries, visit help.riscv.org or email us at help@riscv.org.

riscv.org