News from TSC, ARC, ICs, HCs, SIGs and TGs

Technical Steering Committee (TSC)

Post Ratification Specification Clarification

It was noted that the post-ratification clarification procedure for specifications should be reviewed and clarified. TSC Chairs and Krste Asanovic provided the text, which was reviewed during the last Technical Committee Chair Coordination Meeting held on April 17th, 2024.

The following is the current version of the clarification that will soon be incorporated into the appropriate policies:

Review and Assessment of Motivations for Post-Ratification Changes:

- This includes changes before a new ratified extension is merged into one of the consolidated architecture manuals (e.g. the Unprivileged and Privileged ISA manuals), as well as afterwards.

  Note: Currently only the two ISA manuals exist as consolidated architecture manuals. Other manuals for Non-ISA extensions are expected to eventually be created.

- Architecture extensions have a two-part version number of the form vX.Y (e.g. v1.0 or v1.1), where the vX.0 version is the initial ratified spec, and approved changes become part of a vX.Y version.

  Note: Approved changes that are incorporated into a spec before it is merged into a consolidated architecture manual will be considered part of the official vX.0 spec that is published to the world. (Going forward it is expected that this interval of time between ratification and merge/publish will be small.)

- The TG (Task Group) responsible for an architecture extension, or the owner and governing IC/HC (ISA/Horizontal Committee) for an FT (Fast Track), must thoroughly review the issues prompting the proposed changes and arrive at a consensus on their resolution.

- In general only formatting, text, figure/diagram, pseudocode, and semantic clarifications and corrections may be made to the initial ratified v1.0 spec. Updated specs will be numbered "v1.Y".

Note that semantic corrections only include cases where the semantics were found to be undefined, ambiguous, or impractical to implement (e.g. cases where it is highly unlikely an actual implementation would be affected by the correction, or the correction is backward compatible).

The same constraints apply to a ratified v2.0 spec and the numbering of updates to that spec as "v2.Y" (and in general to a ratified vX.0 spec and numbered vX.Y updates).

Note that a number of changes may be grouped together to produce one updated v1.Y spec that is published (and hence for there to be very few published versions of a ratified spec - ideally just one or two).

- Any changes that are of a more significant nature (e.g. adding new functionality or substantially changing the semantics of existing functionality) must be pursued as a separate new "add-on" architecture extension. (In an extreme case, this may even be a replacement extension that reuses the existing opcodes/CSRs.)

- The final proposed changes and the motivation for them, should be submitted to the relevant IC/HC and then the ARC for final reviews of the changes (and their motivations) as being appropriate resolutions to the instigating issues.

- If it is believed that a "significant" change must be made to the original architecture extension (which would be a very unusual and unfortunate situation), then consideration and evaluation of this requires direct involvement from first the relevant IC/HC and then the Architecture Review Committee (ARC) to determine an appropriate course of action. Any "significant" change to a ratified spec will typically also require engaging with the broader community to assess potential impacts, and ultimately notification to the TSC (so that it can weigh in if it chooses).

Tagged Release Preparation:

- Once the changes are approved, a tagged release of the updated specification should be prepared (with an appropriate new vX.Y version number).

  The tag of a release, to be self-descriptive, should include the spec name and the version number.

Communication and Implementation Plan:

- The finalized release should be announced via GitHub and communicated across the TG, associated ICs/HCs, any other pertinent email lists related to this architecture extension, tech-announce, and help@riscv.org.

Architecture Review Committee (ARC)

Meeting Minutes

The latest ARC meeting minutes is available can be found in the link below:

- 2024-04-16: https://lists.riscv.org/g/tech-unprivileged/message/808

ISA Infrastructure HC

SAIL

There is a lot of activity in the RISC-V Sail model. Here are some of the recent changes:

- **Zcb support merged onto main**. Support for the Zcb extension has been merged on the main branch of the RISC-V Sail model. Martin Berger (Codasip) implemented the Zcb instructions (c.lbu, c.lhu, c.lh, c.sb, c.sh, c.zextb, c.sextb, c.zexth, c.sexth, c.sextw, c.zextw, c.not, c.mul). You can find the PR here.
- **CSR MCONFIGPTR added to model**. Dan Smathers (Seagate) added the CSR MCONFIGPTR to the model. However, initialization of the register still needs to be added. You can find the PR here.
- **Add missing check for RV64 on float conversion instructions**. During a visual inspection of some floating point code, Tim Hutt (Codasip) noticed a missing RV64 check for some double precision instructions. A small PR was generated and approved to fix this. You can find the PR here.
- **Compiler warnings fixed for V-extension**. A number of compiler warnings centered around the Vector extension code were fixed. Ved Shanbhogue (Rivos) identified and fixed the warnings. You can find the PR here.

Documentation

Documentation SIG

With the recent integration of all ratified specifications into the Unprivileged and Privileged specs, the processes surrounding documentation have come into focus. With this in mind, a formal Documentation Special Interest Group (SIG) has been formed, and the inaugural meeting took place on Tuesday, April 23rd. Kevin Broch from Rivos is chairing the SIG.

On Friday, April 12th, PDFs of the Unprivileged and Privileged specifications were distributed internally for review. Issues have been collected via email and the GitHub issue tracker and are currently being addressed. Look for the final publication of the specifications shortly.

You can join in discussions in the Doc SIG mailing list and in the Doc requirements GitHub repo.

News from the CTO Office

Meeting Naming Convention

To make it easy to identify meetings in the public technical calendar, the following meeting naming convention will be adopted: **RV + [MEETING TITLE] + [SIG, TG, etc.]**.

Where:

- RV is the prefix used to identify the meeting as associated with the RISC-V organization. This aids in recognition and helps Members differentiate these meetings in their personal calendars.
- [MEETING TITLE] specifies the focus of the meeting, allowing participants to quickly grasp the agenda or topic.
- [SIG, TG, etc.] denotes the type of group or committee hosting the meeting.

Examples:

- RV Toolchains SIG, RV Golden Model TG, RV Vector SIG

NOTE	Do not add meeting at the end of the meeting title. If you are a meeting host within RISC-V International, please update your meeting tittle as soon as possible.

Groups

Recently Approved Groups

The Technical Steering Committee approved the formation of the Server Platform Task Group. The Server Platform Task Group shall define a specification for a standardized set of hardware and software capabilities, that portable system software (such as operating systems and hypervisors) can rely on being present in a RISC-V server platform. The group will be chaired by Andrei Warkentin (Intel) as Chair and Drew Jones (Ventana Micro Systems) as Vice-Chair. More details about the group can be found here. Their next step is to complete the development of their charter and plan the roadmap, which will then be reviewed and evaluated by the Chairs.

Open Call for Candidates

TSC Elected Representatives

We are halfway to the deadline to apply to represent your constituency on the Technical Steering Committee. If you or someone you know is interested, please ensure the nominations are submitted by the close of business on Tuesday, April 30, 2024. The link to the announcement can be found here and the nomimantions can be made here.

ISA and Horizontal Committee Nominations

We have reached the halfway point in our 2024 Call for Candidates for the ISA and Horizontal Committee chair positions. If you or someone you know is interested, please ensure the nominations are submitted by the close of business on Friday, May 3rd, 2024. The link to the announcement can be found here and the nominations should be made by sending an email to help@riscv.org.

Call for Candidates for SIGs and TGs

SIGs

- AI/ML

- Architectural Compatibility Test

- Automotive

- Datacenter

- Floating Point

- QEMU

- Vector

TGs

- Performance Events

- Packed SIMD

If you want to nominate yourself or someone else, please email **help@riscv.org**.

Extensions

Under Public Review

- E-Trace Encapsulation. End date **May 10, 2024**. The link to the announcement can be found here.

Public Review Recently Completed

- Pointer Masking (J). End date **Apr 19, 2024**. The link to the announcement can be found here.

- Resumable Non-maskable Interrupts. End date **Apr 19, 2024**. The link to the announcement can be found here.

- Shadow Stacks and Landing Pads. End date **Apr 27, 2024**. The link to the announcement can be found here.

Recently Ratified

- B Extension Components (Zba,Zbb,Zbs). PDF. Ratification Date: **Apr 25, 2024**.

- A Extension Components (Zaamo,Zalrsc). PDF. Ratification Date: **Apr 25, 2024**.

- Byte and Halfword Atomic Memory Operations (Zabha). PDF. Ratification Date: **Apr 25, 2024**.

Active Votes

TSC

- **Send RAS Error Record Interface (RERI) Non-ISA specification to the Board of Directors for ratification**. Jira. End date: **2024-05-03**. The link to the text of the voting can be found here. The OpaVote can be found here.

- **Send Eliding Memory-management Fences ISA specification (Svvptc) to the Board of Directors for Ratification**. Jira. End date: **2024-05-09**. The link to the text of the voting can be found here. The OpaVote can be found here.

- **Send the Quality of Service Identifiers (QoS Ids - Jira) and the Capacity and Bandwidth Controller QoS Register Interface (CBQRI - Jira), respectively ISA Fast-Track and non-ISA specifications, to the Board of Directors for ratification.** End date: **2024-05-10**.The link to the text of the voting can be found here. The OpaVote can be found here.

- **TSC vote for approval of the updated charter of the Platform Runtime Services Task Group**. Jira. End date: **2024-05-08**. The link to the text of the voting can be found here. The OpaVote can be found here.

- **TSC vote for approval of the new Vice-chair for the S-Mode PMP Task Group**. Jira. End date: **2024-04-30 (still active)**. The link to the text of the voting can be found here. The OpaVote can be found here.

- **TSC Vote for approval of the new vice-chair for the Security Model Task Group**. Jira. End date: **2024-04-30 (still active)**. The link to the text of the voting can be found here. The OpaVote can be found here.

HC & IC Committees

- **Double Trap (Ssdbltrp, Smdbltrp) Fast-Track ISA Freeze**. Jira. End date: **2024-05-03**. The link to the text of the voting can be found here. The OpaVote can be found here.

Technical Resources

New Disclosure Videos Available

We have 2 new AI-generated disclosure videos available at **Lead/Host Meetings** under tech.riscv.org. Ensure you bookmark it for quick access during meetings. Also, you can access them directly here.

One-stop-shop for Technical Resources

The tech.riscv.org page is your one-stop-shop for all RISC-V technical content. Bookmark it!

Active ICs, HCs, SIGs and TGs

You can find the list of active ICs, HCs, SIGs and TGs at tech.riscv.org/groups.

Extensions Under Development

The status of extensions under development is available at tech.riscv.org/extensions.

Software Ecosystem Dashboard

The Software Ecosystem Dashboard is available at tech.riscv.org/software-ecosystem.

Technical Meetings Calendar Adjusted to Your Local Time Zone

The **RISC-V Technical Meetings Calendar** is available in your own timezone here.

Etherpad

Etherpad, a real-time browser-based editor where users can co-edit documents instantly, is available. No login needed. Etherpad should not store permanent content. To access Etherpad, click on the here. Pads are reusable, so feel free to use the same pad for multiple meetings.

Technical Sessions

Next Technical Session

The next Technical Session entitled "RISC-V Cores in Industrial Quality and Open Source" is scheduled for **May 2, 2024**. It will be held at 7:00 AM Pacific Time and will be presented by **Flo Wohlrab - CEO of OpenHW Group**. You can register for the session here.

Recent Technical Sessions

Profiles: A Historical Perspective

Mark Himelstein, CTO of RISC-V International, presented a technical session on the historical perspective of the RISC-V Profiles. The session was recorded and is now available on YouTube. You can watch it here. This is great resource for those who want to learn more about the RISC-V Profiles and participate in its development and evolution via the recently approved Profiles SIG (Jira).

Tech Sessions on YouTube

We are uploading all Technical Sessions to the RISC-V YouTube channel. You can find the playlists for the 2023 Sessions here. The 2024 Sessions are available here.

Upcoming Events

- RISC-V Summit Europe. June 24-28, 2024, Munich, Germany.
- Hot Chips 2024. August 25-27, 2024. Memorial Auditorium, Stanford University, Stanford, California, USA.
- Open Source Summit Europe. September 16-18, 2024, Vienna, Austria.
- RISC-V Summit North America. October 22-23, 2024, Santa Clara, California, USA.

Past Events

OSS North America 2024

All the recording from OSS North America 2024 are available on the Linux Foundation YouTube Channel. The presentations are available on the here (you need to click on the session to locate the file).

Glossary

- **TSC**: Technical Steering Committee
- **ARC**: Architectural Review Committee
- **IC**: ISA Committee
- **HC**: Horizontal Committee
- **SIG**: Special Interest Group
- **TG**: Task Group

Newsletter Contributions

To submit a topic for the Technical Newsletter, click here. Be sure to carefully read the submission guidelines!

Contact Information

For any queries, visit help.riscv.org or email us at help@riscv.org.

riscv.org