
News from TSC, ARC, ICs, HCs, SIGs and TGs

Technical Steering Committee (TSC)

Post Ratification Specification Clarification

It was noted that the post-ratification clarification procedure for specifications should be reviewed and clarified. TSC Chairs and Krste Asanovic provided the text, which was reviewed during the last Technical Committee Chair Coordination Meeting held on April 17th, 2024.

The following is the current version of the clarification that will soon be incorporated into the appropriate policies:

Review and Assessment of Motivations for Post-Ratification Changes:

- This includes changes before a new ratified extension is merged into one of the consolidated architecture manuals (e.g. the Unprivileged and Privileged ISA manuals), as well as afterwards.

Note: Currently only the two ISA manuals exist as consolidated architecture manuals. Other manuals for Non-ISA extensions are expected to eventually be created.

- Architecture extensions have a two-part version number of the form $vX.Y$ (e.g. $v1.0$ or $v1.1$), where the $vX.0$ version is the initial ratified spec, and approved changes become part of a $vX.Y$ version.

Note: Approved changes that are incorporated into a spec before it is merged into a consolidated architecture manual will be considered part of the official $vX.0$ spec that is published to the world. (Going forward it is expected that this interval of time between ratification and merge/publish will be small.)

- The TG (Task Group) responsible for an architecture extension, or the owner and governing IC/HC (ISA/Horizontal Committee) for an FT (Fast Track), must thoroughly review the issues prompting the proposed changes and arrive at a consensus on their resolution.
- In general only formatting, text, figure/diagram, pseudocode, and semantic clarifications and corrections may be made to the initial ratified $v1.0$ spec. Updated specs will be numbered " $v1.Y$ ".

Note that semantic corrections only include cases where the semantics were found to be undefined, ambiguous, or impractical to implement (e.g. cases where it is highly unlikely an actual implementation would be affected by the correction, or the correction is backward compatible).

The same constraints apply to a ratified v2.0 spec and the numbering of updates to that spec as "v2.Y" (and in general to a ratified vX.0 spec and numbered vX.Y updates).

Note that a number of changes may be grouped together to produce one updated v1.Y spec that is published (and hence for there to be very few published versions of a ratified spec - ideally just one or two).

- Any changes that are of a more significant nature (e.g. adding new functionality or substantially changing the semantics of existing functionality) must be pursued as a separate new "add-on" architecture extension. (In an extreme case, this may even be a replacement extension that reuses the existing opcodes/CSRs.)
- The final proposed changes and the motivation for them, should be submitted to the relevant IC/HC and then the ARC for final reviews of the changes (and their motivations) as being appropriate resolutions to the instigating issues.
- If it is believed that a "significant" change must be made to the original architecture extension (which would be a very unusual and unfortunate situation), then consideration and evaluation of this requires direct involvement from first the relevant IC/HC and then the Architecture Review Committee (ARC) to determine an appropriate course of action. Any "significant" change to a ratified spec will typically also require engaging with the broader community to assess potential impacts, and ultimately notification to the TSC (so that it can weigh in if it chooses).

Tagged Release Preparation:

- Once the changes are approved, a tagged release of the updated specification should be prepared (with an appropriate new vX.Y version number).

The tag of a release, to be self-descriptive, should include the spec name and the version number.

Communication and Implementation Plan:

- The finalized release should be announced via GitHub and communicated across the TG, associated ICs/HCs, any other pertinent email lists related to this architecture extension, tech-announce, and help@riscv.org.

Architecture Review Committee (ARC)

Integration of New Extensions into ISA/Non-ISA Manuals Going Forward

From Greg Favor, Chair of the Technical Steering Committee and Chair of the Privileged ISA Committee, on behalf of the Architecture Review Committee (ARC):

May 28th, 2024

All,

In response to some recent initial confusion, the ARC wants to clarify the intentions going forward for how new architecture extension specs are developed and managed (as part of the move to integrated asciidoc ISA manuals).

Now that we have integrated Unpriv and Priv ISA manuals that contain all ISA extensions (and similar efforts remain for Non-ISA extensions), the intent is for the "arch spec" of future new extensions to not simply be created as a github PR adding a separate new standalone chapter to one of the ISA manuals. Instead, for extensions that affect other existing chapters of the manuals (e.g. adding new bits to existing CSRs or adding on adjunct directly-related functionality), additional PRs will also be created - as part of the extension's overall spec - that update these affected chapters in a more integrated manner. In short, the specs for future extensions will be drafted as a set of PRs on the integrated ISA manuals and on affected Non-ISA spec documents.

The result will be that reviewers of the extension's arch spec will be able to see the "whole picture" as to how an extension affects existing parts of the architecture, and see the spec in its final integrated form. And then, when the extension is ratified, it will be a simple matter of merging these PRs into the ISA/Non-ISA manuals (with any post public review updates incorporated).

A current example of this (that is still working its way through the process towards ratification) is the small group of Double Traps extensions - which contain parts that will reside in the Debug spec and in Priv ISA chapters. Which has raised a question around ratification of the Debug 1.0 spec and whether the whole Debug 1.0 document (including the small addition of the Smdbltrp extension) will be ratified together. And the answer is No. The document as a whole is not being ratified. It is Debug 1.0 that is being ratified. The document will be used as Debug 1.0 goes through public review and other steps of the process - with clear delineation of what parts of the document are and are not part of the Debug 1.0 ratification package. Similarly, when the Double Traps extensions go through the public review/etc. steps to ratification, a clear delineation will be provided as to what parts of the Debug document and the Priv ISA manual are part of this ratification package.

Even the Priv 1.13 extensions are a simple example of this - where only certain chapters of the Priv ISA manual will be part of this ratification package.

The same general idea will apply for all new arch extensions going forward.

Greg

June 12th, 2024

Following (on behalf of the ICs) are some additional comments/clarifications to the email sent out a couple of weeks ago:

First, keep in mind that going forward - with integrated manuals - a new arch extension (or group of related arch extensions) will be mixed in with other extensions in the relevant manual, some of which are already ratified and some of which are concurrently in development or heading towards ratification.

As a written arch spec is being developed, the owners/authors may choose the best approach or written form for its development up til the point of creating a Stable spec that is suitable for sending out for the Internal Review phase of development.

From Internal Review onwards (i.e. for this and all the subsequent broad reviews by IC/HC committees, the ARC, and public review), the arch spec is expected to be in the form of PRs on the integrated ISA manuals - as described in the prior email (below). Logistically this should be done in the form of a branch as part of the riscv-isa-manual repository on GitHub. For Non-ISA arch extensions, until integrated Non-ISA manuals are created, the arch spec will need to be in the form of a standalone GitHub repository.

A fully integrated form of the arch extension spec can then be provided for all broad reviews starting with Internal Review. Review documentation should clearly describe the main chapter for the arch extension and all sundry pieces appearing in other existing chapters. (The arch extension's main chapter should also be cross referencing the sundry pieces of arch functionality that are described elsewhere (and where). For example, any new `*envcfg`, `mseccfg`, or `*stateen` bits.)

Similarly, for spec documents/manuals that contain a mixture of ISA and Non-ISA extensions, and/or a mixture of already ratified parts, new parts that are part of the current ratification package, and other new parts that will be part of other ratification packages, the review documentation for a given ratification package should clearly describe what parts of the spec document/manual are part of this ratification package (and hence up for review).

Lastly, note that the version of the spec document/manual used for reviews should not contain the PRs for other unrated arch extensions that are concurrently making their way through their own development cycle. It should only contain ratified arch extensions and the new arch extension (and any not yet ratified extension that the new extension extension will be dependent and will be ratified ahead of the new extension).

Greg

Documentation

Documentation SIG

The Docs team made several updates over the last couple of weeks. The first is the updated [Glossary](#). Always a work in progress, you can contribute by creating an issue in the [glossary repo](#).

The second is a start on a [Words usage page](#). This page is not finalized and is expected to change. You can contribute to this page by creating an issue in the [Dev guide repo](#).

Tech News

CHERI Alliance Formed to Promote Memory Safety and Software Compartmentalization

Initial members join CHERI Alliance to drive adoption of memory safety and scalable software compartmentalization. Founding members include Capabilities Limited, Cudasip, the FreeBSD Foundation, lowRISC, SCI Semiconductor, and the University of Cambridge.

For more information can be found in [this link](#).

Meeting Naming Convention

To make it easy to identify meetings in the [public technical calendar](#), the following meeting naming convention will be adopted: **RV + [MEETING TITLE] + [SIG, TG, etc.]**.

Where:

- RV is the prefix used to identify the meeting as associated with the RISC-V organization. This aids in recognition and helps Members differentiate these meetings in their personal calendars.
- [MEETING TITLE] specifies the focus of the meeting, allowing participants to quickly grasp the agenda or topic.
- [SIG, TG, etc.] denotes the type of group or committee hosting the meeting.

Examples:

- RV Toolchains SIG, RV Golden Model TG, RV Vector SIG

NOTE

Do not add meeting at the end of the meeting title. If you are a meeting host within RISC-V International, please update your meeting title as soon as possible.

Nominations are open to represent RISC-V member elected representatives on the RISC-V Board of Directors

Nominations are open to represent RISC-V member elected representatives on the RISC-V Board of Directors. We invite members to participate in RISC-V governance as outlined in our governing documents as well as through our many RISC-V committees and groups. All RISC-V members have a voice on the Board.

Nominations are welcome until 5pm ET on June 22, 2024.

Currently, there are:

- 6 Nominees for Director representatives for Premier TSC & Strategic members
- 2 Nominees for Director representative for Community Organization members
- 3 Nominees for Director representative for Community Individual members

Any member in good standing may self-nominate [using the online form](#), and candidates will be featured on our [2024 Elections website page](#).

Groups

TSC Strategic Member Representative Election

The TSC Strategic Member Representative Election has closed. Here are the results:

Candidate	Count
Jianying Peng, Nuclei System Technology Co.	14
Ken Dockser, Tenstorrent	29
Roger Espasa, Semidynamics	26

The incumbents, Ken Dockser and Roger Espasa, were re-elected to represent Strategic member companies for a term which runs from July 1, 2024, to July 1, 2025.

There were 41 votes for 167 ballots (25%) cast.

TSC Community/Individual Member Election

The TSC Community/Individual Member Election has closed. Here are the results:

Candidate	Count
Cathy Lee	112
Guy Lemieux	266
Abstain	16

There were 394 votes for 4204 valid ballots (9.4%) voted.

The member elected for a term from July 1, 2024, to June 30, 2025, is Guy Lemieux.

Recently Re-elected HCs and ICS Chairs and Vice-Chairs by the TSC

Committee	Chair	Vice-Chair
Unprivileged ISA Committee	Krste Asanović	Earl Killian
Privileged ISA Committee	Greg Favor	Andrew Waterman
Apps & Tools SW Horizontal Committee	Philipp Tomsich	David Chen
SOC Infra Horizontal Committee	Ved Shanbhogue	Gajinder Panesar
Privileged SW Horizontal Committee		John Hengeveld
ISA Infrastructure Horizontal Committee	Wei Wu	Allen Baum
Technology Horizontal Committee	John Leidel	Nambi Ju
Security Horizontal Committee	Andrew Dellow	Ravi Sahita

Open Call for Candidates

Call for Candidates for SIGs and TGs

SIGs

- [Security Response Team](#)

TGs

- [S-mode Physical Memory Protection \(SPMP\)](#)
- [Packed SIMD](#)

If you want to nominate yourself or someone else, please email help@riscv.org.

Extensions

Recently Approved Waivers

The Technical Chairs and Vice-chairs approved the waiver for Priv 1.13. The details can be found [here](#). The OpaVote can be found [here](#).

Recently Ratified

- [RAS Error Record Interface \(RERI\). PDF](#). Ratification Date: **May 23, 2024**.

Upcoming Ratifications

- [Capacity and Bandwidth Controller QoS Register Interface \(CBQRI\)](#). Target Date: **June 27, 2024**.
- [E-Trace Encapsulation](#). Target Date: **June 27, 2024**.
- [Obviating Memory-Management Instructions after Marking PTEs Valid](#). Target Date: **June 27, 2024**.
- [Quality-of-Service \(QoS\) Identifiers](#). Target Date: **June 27, 2024**.
- [Shadow Stacks and Landing Pads](#). Target Date: **June 27, 2024**.
- [Resumable Non-maskable Interrupts](#). Target Date: **June 27, 2024**.

Active Votes

HC & IC Committees

- **Freeze: Control Transfer Register (Smctr, Sctr).** [Jira](#). End date: **2024-06-28**. The link to the text of the voting can be found [here](#). The OpaVote can be found [here](#).
- **Freeze: Priv 1.13 Specification.** [Jira](#). End date: **2024-06-24**. The link to the text of the voting can be found [here](#). The OpaVote can be found [here](#).

Technical Resources

New Disclosure Videos Available

We have 2 new AI-generated disclosure videos available at **Lead/Host Meetings** under tech.riscv.org. Ensure you bookmark it for quick access during meetings. Also, you can access them directly [here](#).

One-stop-shop for Technical Resources

The tech.riscv.org page is your one-stop-shop for all RISC-V technical content. Bookmark it!

Active ICs, HCs, SIGs and TGs

You can find the list of active ICs, HCs, SIGs and TGs at tech.riscv.org/groups.

Extensions Under Development

The status of extensions under development is available at tech.riscv.org/extensions.

Software Ecosystem Dashboard

The Software Ecosystem Dashboard is available at tech.riscv.org/software-ecosystem.

Technical Meetings Calendar Adjusted to Your Local Time Zone

The **RISC-V Technical Meetings Calendar** is available in your own timezone [here](#).

Etherpad

Etherpad, a real-time browser-based editor where users can co-edit documents instantly, is available. No login needed. Etherpad should not store permanent content. To access Etherpad, click on the [here](#). Pads are reusable, so feel free to use the same pad for multiple meetings.

Technical Sessions

Next Technical Session

The next Technical Session entitled "RISC-V Technical Session: Digging for Documentation - A Tale of Reverse Engineering" is scheduled for **June 20, 2024**. It will be held at 7:00 AM Pacific Time and will be presented by **Daniel Maslowski - Software Engineer at IAOTAI**. You can register for the session [here](#).

Tech Sessions on YouTube

We are uploading all Technical Sessions to the RISC-V YouTube channel. You can find the playlists for the 2023 Sessions [here](#). The 2024 Sessions are available [here](#).

Upcoming Events

- [RISC-V Summit Europe](#). June 24-28, 2024, Munich, Germany.
- [Hot Chips 2024](#). August 25-27, 2024. Memorial Auditorium, Stanford University, Stanford, California, USA.
- [Open Source Summit Europe](#). September 16-18, 2024, Vienna, Austria.
- [RISC-V Summit North America](#). October 22-23, 2024, Santa Clara, California, USA.

Glossary

- **TSC:** Technical Steering Committee
- **ARC:** Architectural Review Committee
- **IC:** ISA Committee
- **HC:** Horizontal Committee
- **SIG:** Special Interest Group
- **TG:** Task Group

Newsletter Contributions

To submit a topic for the Technical Newsletter, [click here](#). Be sure to carefully read the submission guidelines!

Contact Information

For any queries, visit help.riscv.org or email us at help@riscv.org.

