



Technical Newsletter

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## News from TSC, ARC, ICs, HCs, SIGs and TGs

### Architecture Review Committee (ARC)

The latest ARC meeting minutes, from the meeting held on June 11, 2024, are available [here](#).  
*Contributed by Krste Asanović, SiFive.*

### Unprivileged Spec IC

#### Limitation with Zcmp push/pop instructions and frame pointer

The push/pop instructions in the Zcmp extension are not compatible with the conventional Linux ABI for frame pointer layout. Currently, enabling the frame pointer requires disabling the Zcmp extension, which results in a code size penalty. A frame pointer ensures that a stack backtrace can always be performed. Descriptions of the problem and proposed solutions (add new push/pop, change existing push/pop, or add new ABIs to match existing push/pop) are publicly available.

- [Problem and Proposed Solutions](#)
- [Groups.io Discussions](#)
- [psABI GitHub issue](#)
- [Toolchains and psABI TG meetings](#)

Please join the discussions if you have questions, comments, ideas to contribute, or feel you might be impacted by the proposed solutions. *Contributed by Ana Pazos, Qualcomm.*

# Tech News

## Welcome Message from Andrea Gallo, Vice President of Technology at RISC-V International

*"I am truly excited to be joining your team. I am excited by the fast pace of innovation from all members of this community, I am thrilled because instead of fragmentation we are able to funnel their energy towards evolving common standards that they all adopt and comply with, I am excited because we are driving hardware-design based on software-driven innovation!"*

[Andrea Gallo](#) heads up the Technical Activities at RISC-V International with a mission to facilitate the technical vision, cultivate stakeholder engagement, and drive strategy in deeply engaged collaboration with RISC-V members across workgroups and committees, growing the adoption of the RISC-V Instruction Set Architecture. Prior to RISC-V International, Andrea held multiple roles at Linaro, starting all Arm datacenter engineering activities from the ground up, from firmware to complex cloud workloads. Later, as VP of Segment Groups, he oversaw verticals from IoT to HPC, including smartphones and AI/ML. In his last years at Linaro, he served as Executive VP of Business Development, managing all membership contracts and starting new collaborative projects from automotive to Windows on Arm. Prior to Linaro, Andrea was a Fellow at ST-Ericsson for smartphones and application processors and served as the first member representative in the Linaro TSC. Over the years at STMicroelectronics, he consistently led the optimization of hardware-software architectures for new ICs and set up remote teams in India. Andrea holds a University Degree in Telecommunications and speaks fluent French and English, in addition to his native Italian.

Andrea may be reached at [andrea@riscv.org](mailto:andrea@riscv.org).

## Award Recipients at RISC-V Summit Europe 2024

During the RISC-V Summit Europe 2024, held in Munich, Germany, from June 24-28, 2024, the following individuals were recognized for their contributions to the RISC-V community:

### Technical Leadership Awards

- Yungang Bao, Chief Scientist - Beijing Institute of Open Source Chip
- Richard Newell, Associate Technical Fellow - Microchip Technology

### Technical Contributor Awards

- Paul Ku, Deputy Technical Director - Andes Technology
- Ken Dockser, Senior Principal Architect - Tenstorrent
- Beeman Strong, Principal Engineer - Rivos, Inc.

## **Board of Directors Software Leadership Award**

- Nathan Egge, Staff Software Engineer - Google Android

## **Board of Directors Software Contributor Award**

- Europe: Alex Bradbury - Igalia
- Asia: Chunqiang Li - Alibaba
- Americas: Andrew Jones - Ventana Micro Systems

Thank you for your incredible contributions, collaboration, and leadership in the RISC-V community.

# Extensions

## Recently Approved Waivers

The Technical Chairs and Vice-chairs approved the waiver for Priv 1.13. The details can be found [here](#). The OpaVote can be found [here](#).

## Recently Ratified

- [Capacity and Bandwidth Controller QoS Register Interface \(CBQRI\)](#), led by Ved Shanbhogue under the governance of the SOC Infrastructure Horizontal Committee.
- [E-Trace Encapsulation](#), led by Iain Robertson under the governance of the SOC Infrastructure Horizontal Committee
- [Obviating Memory-Management Instructions after Marking PTEs Valid](#), led by Ved Shanbhogue under the governance of the Privileged Specification ISA Committee.
- [Quality-of-Service \(QoS\) Identifiers](#), led by Ved Shanbhogue under the governance of the Privileged Specification ISA Committee.
- [Shadow Stacks and Landing Pads](#), led by Ved Shanbhogue and Georgios Christou under the governance of the Unprivileged Specification ISA Committee.
- [Resumable Non-maskable Interrupts](#), led by Andrew Waterman and Ved Shanbhogue under the governance of the Privileged Specification ISA Committee.
- [BF16 Extensions](#), led by Ken Dockser under the governance of the Unprivileged Specification ISA Committee.

# Technical Resources

- [Meeting Disclosure Videos Available](#)
- [One-stop-shop for Technical Resources](#)
- [Active ICs, HCs, SIGs and TGs](#)
- [Extensions Under Development](#)
- [Software Ecosystem Dashboard](#)
- [Technical Meetings Calendar Adjusted to Your Local Time Zone](#)
- [Etherpad](#)

# Technical Sessions

## Tech Sessions on YouTube

We are uploading all Technical Sessions to the RISC-V YouTube channel. You can find the playlists for the 2023 Sessions [here](#). The 2024 Sessions are available [here](#).

# Upcoming Events

- [Hot Chips 2024](#). August 25-27, 2024. Memorial Auditorium, Stanford University, Stanford, California, USA.
- [Open Source Summit Europe](#). September 16-18, 2024, Vienna, Austria.
- [RISC-V Summit North America](#). October 22-23, 2024, Santa Clara, California, USA.

# Glossary

- **TSC:** Technical Steering Committee
- **ARC:** Architectural Review Committee
- **IC:** ISA Committee
- **HC:** Horizontal Committee
- **SIG:** Special Interest Group
- **TG:** Task Group

## Newsletter Contributions

To submit a topic for the Technical Newsletter, [click here](#). Be sure to carefully read the submission guidelines!

## Contact Information

For any queries, visit [help.riscv.org](https://help.riscv.org) or email us at [help@riscv.org](mailto:help@riscv.org).

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