

Technical Newsletter 2024-08-23 Volume: 18

News from TSC, ARC, ICs, HCs, SIGs and TGs

Technical Steering Committee (TSC)

A table detailing all extensions that are part of RVA23 and RVB23 is available here as reference.

Architecture Review Committee (ARC)

The latest ARC meeting minutes, from the meeting held on August 06, 2024, are available here. During that meeting ARC approved the Freezing of the following specifications:

- RVV Intrinsics
- Semihosting

Tech News

Extensions

Recently Approved Plans

The following development plans have been approved by the Technical Chairs:

- IO Mapping Table. Details
- Supervisor Binary Interface 3.0. Details
- Platform Management Interface RPMI. Details

Under Public Review

The following specification is currently under public review:

• RISC-V N-Trace, Trace Control Interface and Trace Connectors. Details

Public Review Recently Completed

The following specification has recently completed public review:

• Control Transfer Records (CTR). Details

Recently Ratified

• Double Trap, led by Ved Shanbhogue under the governance of the Privileged Spec (IC) Committee. The specification can be found here.

Recently Approved Waivers

The Technical Chairs and Vice-chairs approved the waiver for Priv 1.13. The details can be found here. The OpaVote can be found here.

Active Votes

TSC

• Specification Freeze Approvals:

RVA23. End date is September 4, 2024. OpaVote.

RVB23. End date is September 4, 2024. OpaVote.

• Task Group Formation Approvals:

Performance Events Sampling. End date is August 29, 2024. OpaVote.

Memory Tagging. End date is August 29, 2024. OpaVote.

Composable Custom Extensions. End date is August 29, 2024. OpaVote.

Dev Partners

With the participation of JIA Wei from the RISC-V Development Partner, PLCT, the Zimop/Zcmop extensions ("May Be Ops") has successfully merged gcc patches upstream: commit.

Dev Labs

The PLCT (Programming Language and Compiler Technology) Lab at the Institute of Software, Chinese Academy of Sciences (ISCAS) has officially met the criteria of the RISC-V Ecosystem Labs Program and is now the second partner to be fully certified and authorized to display the program's logo.

As a founding member of the RISC-V Labs program, PLCT has provided public sandboxes and CI infrastructure for several years through their RISC-V Lab at PLCT for several years.

For more details on available cloud resources or to learn about becoming a Lab Partner, visit the RISC-V Labs and Lab Partner pages.

Events

RISC-V Tech Sessions

The next RISC-V Tech Sessions entitled "ConvBench: Benchmark for 2D Convolution Primitive Evaluation" will be held on August 29, 2024. The session will be held at 7:00 AM PDT. Register here.

Upcoming Events

- Hot Chips 2024. August 25-27, 2024. Memorial Auditorium, Stanford University, Stanford, California, USA.
- Open Source Summit Europe. September 16-18, 2024, Vienna, Austria.
- RISC-V Summit North America. October 22-23, 2024, Santa Clara, California, USA.

Resources

- Official RISC-V Website
- RISC-V YourTube Channel
- Meeting Disclosure Videos Available
- One-stop-shop for Technical Resources
- Active ICs, HCs, SIGs and TGs
- Extensions Under Development
- Software Ecosystem Dashboard
- Technical Meetings Calendar Adjusted to Your Local Time Zone
- Etherpad

Glossary

- TSC: Technical Steering Committee
- ARC: Architectural Review Committee
- IC: ISA Committee
- HC: Horizontal Committee
- SIG: Special Interest Group
- TG: Task Group

Newsletter Contributions

To submit a topic for the Technical Newsletter, click here. Be sure to carefully read the submission guidelines!

Contact Information

For any queries, visit help.riscv.org or email us at help@riscv.org.



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