Recently Ratified Extensions

If you are looking for documentation on a recently ratified extension that has not yet been merged into the published specifications listed on the RISC-V Specifications page, check the table below. These extensions are completely ratified by RISC-V and will be merged into the final specifications in the coming months.

Specification name	Ratification date	New extension(s)
Zmmul Extension	June 2022	Zmmul
PMP Enhancements for memory access and execution prevention on Machine mode (Smepmp)	November 2021	Smepmp
RISC-V Base Cache Management Operation ISA Extensions	November 2021	Zicbom, Zicbop, Zicboz
RISC-V Bit-Manipulation ISA-extensions	November 2021	Zba, Zbb, Zbc, Zbs
RISC-V Count Overflow and Mode-Based Filtering Extension	November 2021	Sscofpmf
RISC-V Cryptography Extensions Volume I: Scalar & Entropy Source Instructions	November 2021	Zbkb, Zbkc, Zbkx, Zknd, Zkne, Zknh, Zksed, Zksh, Zkn, Zks, Zkt, Zk, Zkr
RISC-V State Enable Extension	November 2021	Smstateen
RISC-V "stimecmp / vstimecmp" Extension	November 2021	Sstc
RISC-V Vector Extension	November 2021	Zve32x, Zve32f, Zve64x, Zve64f, Zve64d, Zve, Zvl32b, Zvl64b, Zvl128b, Zvl256b, Zvl512b, Zvl1024b, Zvl, Zv
The RISC-V Instruction Set Manual Volume II: Privileged Architecture	November 2021	Sm1p12, Ss1p12, Sv57, Hypervisor, Svinval, Svnapot, Svpbmt
"Zfh" and "Zfhmin" Standard Extensions for Half-Precision Floating-Point	November 2021	Zfh, Zfhmin
"Zfinx", "Zdinx", "Zhinx", "Zhinxmin": Standard Extensions for Floating-Point in Integer Registers	November 2021	Zfinx, Zdinx, Zhinx, Zhinxmin