RISC-V extension and feature support in the Open Source SW Ecosystem

This page gives an overview of the extension and feature support in the RISC-V SW ecosystem.

Overview

- This page only tracks ratified extensions and features that are specified by groups (TGs, HCs) of RISC-V International.
- The extensions and features are grouped by their specification's state (published, ratified, frozen).
- Published (official) specifications can be found here: https://riscv.org/technical/specifications/
- The main repository of the ISA specifications is: https://github.com/riscv/riscv-isa-manual
- The following wiki page lists all recently ratified extensions, that are not merged into the ISA specification yet: Recently Ratified Extensions
- The Specification Status lists the specifications that are frozen or ready for ratification

Table description

The subsections below contain tables that summarize the current state of extensions and features. The following description helps to interpret the table cell's contents:

- upstream...SW support has been merged into the main development branch of the corresponding SW project
- staging branch...SW support lives in a staging branch and is not upstreamed
- PR...SW support exists in form of a pull request for upstream (in-review or waiting for ratification)
- n/a...not applicable, not relevant, or not required
- missing...currently no known implementation
- dev:X...feature is in development by X
- empty cells...unknown status (feel free to share your knowledge)

ISA extension naming conventions

This is just a summary of the naming convention as defined in the unpriv specification.

ISA extension description example: RV64I1p0M1p0A1p0F1p0D1p0 or RV32I2_M2_A2 (P extension requires underscore!)

Prefixes:

- Extensions with prefix Z...standard user-level
- Extensions with prefix X...non-standard user-level
- Extensions with prefix S...standard supervisor-level
- Extensions with prefix SX...non-standard supervisor-level

Published specifications (20191213)

- The RISC-V Instruction Set Manual, Volume I: User-Level ISA, Document Version 20191213
- The RISC-V Instruction Set Manual, Volume II: Privileged Architecture, Document Version 20190608-Priv-MSU-Ratified

The table below lists the status of the extensions and features of above listed published extensions.

Extension	Spike	Qemu	Binutils	GCC	glibc	newlib	LLVM	OpenSBI	FreeBSD	Linux kernel	GDB
RV32I	upstream	upstream	upstream	upstream	upstream	upstream	upstream	upstream	not supported	upstream	upstream
RV64I	upstream	upstream	upstream	upstream	upstream	upstream	upstream	upstream	upstream	upstream	upstream
Big-endian support	upstream			upstream			not supported		not supported		upstream
M (Multiplication and Division)	upstream	upstream	upstream	upstream	n/a	n/a	upstream	n/a	n/a	n/a	upstream

A (Atomic)	upstream	upstream	upstream	upstream	n/a	n/a	upstream	upstream (atomics)	upstream (atomics)	upstream (atomics)	upstream
F (SP float)	upstream	upstream	upstream	upstream	upstream	upstream	upstream		upstream	upstream	upstream
D (DP float)	upstream	upstream	upstream	upstream	upstream	upstream	upstream		upstream	upstream	upstream
Q (QP float)			upstream				not supported		not supported		upstream
RVWMO	upstream (emulation is seq. consistent)	upstream (emulation is seq. consistent)	n/a	n/a	n/a	n/a	n/a	upstream (barriers and locks)	upstream (barriers and locks)	upstream (barriers and locks), but needs optimization	upstream
C (compressed)	upstream	upstream	upstream	upstream	n/a	n/a	upstream		upstream	upstream	
Zifencei	upstream	upstream	upstream	upstream			not supported		upstream	upstream	
Machine ISA: CSRs	upstream	upstream	upstream						n/a		
Machine ISA: ECALL, EBREAK	upstream	upstream							upstream	upstream	
Machine ISA: MRET/SRET /URET	upstream	upstream							n/a		
Machine ISA: WFI	upstream	upstream							upstream	upstream	
Machine ISA: PMP									n/a		
Supervisor ISA: CSRs	upstream	upstream							upstream		
Supervisor ISA: SFENCE.VMA	upstream	upstream							upstream	upstream	
Supervisor ISA: Sv32, Sv39, Sv48	upstream	upstream							Sv39 upstream	upstream (sv39)	

Unpublished ratified extensions

Extensions and features in the table below are ratified, but not published in a consolidated RISC-V ISA specification document.

Extension	Spike	Qemu	Binutils	GCC	glibc	newlib	LLVM	OpenSBI	FreeBSD	Linux kernel	GDB
Zihintpause	upstream	Mailpatch	upstream				upstream				
Vector: Zvamo, Zvlsseg, Zvediv, Zvqmac, Zve32x, Zve32f, Zve64x, Zve64f, Zve64d, Zvfh, Zve	upstream	upstream	upstream	rvv-next branch			upstream	upstream (experimental,FP16 ABI not settled)	not supported		
Bitmanip: Zba, Zbb, Zbc, Zbs	upstream	upstream	upstream	PR	dev branch		upstream	upstream (experimental)	not used		
FP in INT regs: Zfinx	PR	upstream	upstream(Zfinx, Zdinx)	Mailpatch (Zfinx,Zdinx)			MC upstream		not supported		
Half Width FP: Zfh, Zfhmin	upstream	upstream	upstream (Zfh only) Mailpatch (Zfhmin)				upstream		not supported		
ePMP: Smepmp	upstream	upstream (but 0.9.3)	upstream (CSR only; part of Priv 1.12 support)				PR		not supported		
Scalar crypto: Zbkb, Zbkc, Zbkx, Zknd, Zkne, Zknh, Zksed, Zksh, Zkn, Zks, Zkt, Zk, Zkr	upstream	upstream	upstream	upstream(only minimal support and wait c-api merge)			upstream		not used		
Priv 1.12: Sm1-12, Ss1-12, Sv57		upstream	upstream						not supported		

CMO base: Zicbom, Zicbop, Zicboz	upstream	Mailpatch	upstream				PR,PR		not supported		
Hypervisor: H	upstream	upstream	upstream (except handling as 'H' extension; now a part of 'I' extension)	n/a	n/a	n/a		upstream	not supported	upstream (5.16)	
State Enable: Smstateen	upstream	Mailpatch	Mailpatch						not supported		
Time compare: Sstc		Mailpatch	Mailpatch						not supported		
Counter overflow and filtering: Sscofmpf	PR	Mailpatch	Mailpatch						not supported		
Fast TLP invalidation: Svinval	upstream	upstream	upstream						not supported		
NAPOT pages: Svnapot	upstream	upstream							not supported		
Page-based memory types: Svpbmt	upstream	upstream							not supported		
Code Size Reduction: Zcee	dev branch	dev branch	dev branch	dev branch			dev branch		not supported		
Packed SIMD: Zpn, Zpsfoperand, Zprvsfextra	upstream (v0.9.2)	Mailpatch	PR	PR					not supported		
Resumable Non-maskable Interrupts: Smrnmi									not supported		
Core-local Interrupt Controller: CLINT	upstream	upstream							upstream	upstream (clocksource)	
Advanced Core-local Interrupt Controller: ACLINT		upstream							not supported	Patchwork	
Zmmul	upstream	upstream	Mailpatch	Mailpatch			patch		n/a		
Pointer masking: Zjpm									not supported		

Specifications that are at least frozen

Extensions and features in the table below are either frozen or ready-for-ratification.

Extension	Spike	Qemu	Binutils	GCC	glibc	newlib	LLVM	OpenSBI	FreeBSD	Linux kernel	GDB
-none-											

Specifications that are at least stable

Note, that this section only lists specifications that are planned to be released in the near future, but are not frozen yet.

Extension	Spike	Qemu	Binutils	GCC	glibc	newlib	LLVM	OpenSBI	FreeBSD	Linux kernel	GDB
psABI: Standard ABIs: ILP32, ILP32F, ILP32D, LP64, LP64F, LP64D, LP64Q	n/a	n/a	upstream	ilp32, ilp32f, ilp32d, lp64, lp64f, lp64d	ilp32, ilp32d, lp64, lp64d	ilp32, ilp32f, ilp32d, lp64, lp64f, lp64d	ilp32, ilp32d, lp64, lp64d	n/a	lp64, lp64d	n/a	

Specifications that are not stable

Note that this section only exists for historical purposes and the table below is not considered complete. Further, there are no attempts to track the SW support of unstable features here.

Extension	Spike	Qemu	Binutils	GCC	glibc	newlib	LLVM	OpenSBI	FreeBSD	Linux kernel	GDB
Embedded ABI: ILP32E, LP64E	n/a	n/a	upstream	upstream	not supported	upstream	not supported	n/a	n/a	n/a	not supported

Gaps

- Vector Extension Intrinsics (specification exists, but not frozen)
- Vector Calling Convention (specification exists, but not frozen)
- Scalar Crypto Intrinsics