Operating Systems

This page gives an overview of upstream projects. If you miss information or find mistakes, please edit.

Android

- RISC-V Android port home page (GitHub)

Apache NuttX

- NuttX Homepage
- NuttX Source Code (GitHub)

RISC-V Maintainers

NuttX RTOS has a weaker sense of maintainership than many open-source projects. However, the primary contributors are:

- Janne Rosberg (Offcode)
- Masayuki Ishikawa (Sony Corporation)
- Xiang Xiao (Xiaomi Corporation)

FreeBSD

- FreeBSD Homepage
- Upstream wiki page

RISC-V Maintainers

FreeBSD has a weaker sense of maintainership than many open-source projects. However, the primary contributors are:

- John Baldwin (SRI International)
- Ruslan Bukin (University of Cambridge)
- Jessica Clarke (University of Cambridge)
- Mitchell Horne
- Kristof Provost

Releases

FreeBSD major releases are approximately every two years, with minor releases every year and interim security patches as needed.

Previous releases:

- FreeBSD 13.0 (2021-04-13) - RISC-V promoted to being a Tier 2 architecture
- FreeBSD 12.2 (2020-10-27)
- FreeBSD 12.1 (2019-11-4)
- FreeBSD 12.0 (2018-12-11) - RISC-V added as a Tier 3 architecture

RISC-V Status

RV64G is supported for several popular hardware, emulated and FPGA-based platforms as a Tier 2 platform. Various feature additions and performance optimisation opportunities exist. See the upstream wiki page linked above for more details.

FreeRTOS

RISC-V Status

RISC-V support has been merged in FreeRTOS. A couple of boards is directly supported.

Haiku

Haiku has been ported to RISC-V: https://www.haiku-os.org/blog/kallisti5/2021-11-07_booting_our_risc-v_images/

Hubris

There is an initial port of Hubris to the Freedom E310 core on a Sparkfun RED-V board: https://github.com/oxidecomputer/hubris/discussions/365

Note from Cliff:

> In general, Hubris was originally designed with the intent of moving to RISC-V *eventually*, which is part of why we're so register-focused in the calling convention.

Illumos

Illumos has been ported to the Allwinner D1: https://github.com/n-hys/illumos-gate/wiki/Allwinner-D1-Nezha

Linux

RISC-V Maintainers

- Palmer Dabbelt
- Albert Ou
- Paul Walmsley

Releases

The Linux kernel has been merged mainline in the 4.15 merge window in November 2017.

Since then a range of Distributions have RISC-V ports. E.g.:

- Debian
- Fedora
- openSUSE
- Buildroot
- Yocto
- Arch Linux (Install on Unmatched)
- Gentoo Linux
- openEuler
- AOSP for RISC-V 10, AOSP 12 rebasing effort main repos , PLCT wip repos

RISC-V Status

The Linux kernel supports RV64G as well as RV32G.

Oberon

There is an Oberon port for RISC-V, e.g., for the Bouffalo Lab BL808: http://oberon.wikidot.com/project-oberon-v

OpenBSD

Releases

RISC-V Status

Work is in progress adding the port, with the first commit made on 23rd April 2021.

- https://www.openbsd.org/riscv64.html
- https://www.openbsd.org/papers/Porting_OpenBSD_to_RISCV_FinalReport.pdf

Plan 9

Plan 9 ports exist; see also: https://ntnuopen.ntnu.no/ntnu-xmlui/bitstream/handle/11250/2902876/no.ntnu:inspera:74730513:31541262.pdf?sequence=1

xv6

There are multiple RISC-V ports of xv6 (https://pdos.csail.mit.edu/6.828/2022/xv6.html).

- Generic: https://github.com/mit-pdos/xv6-riscv
- Book: https://github.com/mit-pdos/xv6-riscv-book

Ports

- iCE40 FPGA https://gitlab.com/x653/xv6-riscv-fpga
- Allwinner D1: https://github.com/michaelengel/xv6-d1
- JH7110 (VisionFive 2): https://github.com/michaelengel/xv6-vf2

Zephyr

RISC-V Maintainers

- Karol Gugala (Antmicro)
- Tomasz Gorochowik (Antmicro)
- Filip Kokosinski (Antmicro)

Releases

RISC-V support has been present in the Zephyr RTOS since:

- v1.7.0, for RV32I (March 2017)
- v2.0.0, for RV64I (September 2019)
- v3.2.0, for RV32E (September 2022)

RISC-V Status

As of February 2023, dozens of physical (non-emulated) targets are supported in Zephyr.

- List of RISC-V Boards: https://docs.zephyrproject.org/latest/boards/riscv/index.html
- Zephyr release notes: https://docs.zephyrproject.org/latest/releases/index.html