Emulators and Simulators

This page gives an overview of upstream projects. If you miss information or find mistakes, please edit.

QEMU

QEMU is a generic and open source machine emulator and virtualizer.

- QEMU Homepage
- Source Release Page

RISC-V maintainers

- Alistair Francis (WDC)
- Palmer Dabbelt (Google)

Releases

- QEMU 6.0.0 (2021-04-29)
- QEMU 5.2.0 (2020-12-08))
- QEMU 5.1.1 (2020-08-11)
- QEMU 5.0.0 (2020-04-28)

RISC-V status

- RV32GC = RV32IMAFDC is implemented
- RV64GC = RV64IMAFDC is implemented
- Privileged and unprivileged instruction specifications are supported
- RV32E is supported
- RISC-V specific wiki page: https://wiki.qemu.org/Documentation/Platforms/RISCV
- Unratified extension support is kept mainline
    - Vector extension v0.7.1

Spike / riscv-isa-sim

Spike, the RISC-V ISA Simulator, implements a functional model of one or more RISC-V harts.

- Spike github repository

RISC-V status

- Spike has historically been the proof-of-concept target for all RISC-V extensions (it has recently been superseeded by a SAIL generated simulation)
- RV32GC = RV32IMAFDC is implemented
- RV64GC = RV64IMAFDC is implemented
- Additionally: Zifencei, Zicsr
- Q v2.2
- Support for LE and BE
- Spike is sequentially consistent
- Machine, Supervisor, and User modes, v1.11
- Unratified extensions:
    - B (bitmanip) v0.92
    - K (scalar crypto) v0.8.1
    - V (vector) v0.10 with Zvlsseg/Zvamo
    - P (simd) v0.9.2
    - H (hypervisor) v0.6.1
    - Svnapot extension v0.1
    - Debug v0.14