

Ratified Extensions

A general overview and status of various extension which are presently under development can be found at the [Specification Status](#) page.

If you are looking for documentation on a recently ratified extension that has not yet been merged into the published specifications listed at the [RISC-V Specifications](#) page, check the table below. Extensions with hyperlinks reflect specifications which are completely ratified by RISC-V but have not yet been merged into the final specifications.

Specification name	Ratification date	New extension(s) or Profile(s)
RISC-V Supervisor Counter Delegation	March 2024	Smcdeleg, Ssccfg
May-Be-Operations	March 2024	Zimop, Zcmop
RISC-V Indirect CSR Access (Smcsrind/Sscsrind)	February 2024	Smcsrind, Sscsrind
RISC-V Integer Conditional (Zicnd) operations extension	November 2023	Zicnd
Hardware Updating of PTE A/D Bits (Svadu)	November 2023	Svadu
RISC-V Cycle and Instret Privilege Mode Filtering (Smcntrpmf)	November 2023	Smcntrpmf
Atomic Compare-and-Swap (CAS) Instructions (Zacas)	November 2023	Zacas
RISC-V Cryptography Extensions Volume II: Vector Instructions	September 2023	Zvbb, Zvbc, Zvkb, Zvkg, Zvkn, Zvknc, Zvkned, Zvkng, Zvknha, Zvknhb, Zvks, Zvksc, Zvkscd, Zvksg, Zvksh, Zvkt
"Zfa" Standard Extension for Additional Floating-Point Instructions	September 2023	Zfa
RISC-V Advanced Interrupt Architecture	June 2023	Smaia, Ssaia
"Zvfh/Zvfhmin.:" Vector Extension for Half-Precision Floating-Point Arithmetic/Vector Extension for Minimal Half-Precision Floating-Point Arithmetic	June 2023	Zvfh, Zvfhmin
"Zihintntl" Non-Temporal Locality Hints	May 2023	Zihintntl
RISC-V Code Size Reduction	April 2023	Zca, Zcb, Zcd, Zce, Zcf, Zcmp, Zcmt
RISC-V Profiles	March 2023	RVA20, RVI20, RVA22
"Zicntr" and "Zihpm" Counters	March 2023	Zicntr, Zihpm
RV32E and RV64E Base Integer Instruction Sets	January 2023	RV32E/RV64E
"Ztso" Standard Extension for Total Store Ordering	January 2023	Ztso
RISC-V Wait-on-Reservation-Set (Zawrs) extension	November 2022	Zawrs
Zmmul Extension	June 2022	Zmmul
PMP Enhancements for memory access and execution prevention on Machine mode (Smepmp)	November 2021	Smepmp
RISC-V Base Cache Management Operation ISA Extensions	November 2021	Zicbom, Zicbop, Zicboz
RISC-V Bit-Manipulation ISA-extensions	November 2021	Zba, Zbb, Zbc, Zbs
RISC-V Count Overflow and Mode-Based Filtering Extension	November 2021	Sscfpmf
RISC-V Cryptography Extensions Volume I: Scalar & Entropy Source Instructions	November 2021	Zbkb, Zbkc, Zbkx, Zknd, Zkne, Zknh, Zksed, Zksh, Zkn, Zks, Zkt, Zk, Zkr
RISC-V State Enable Extension	November 2021	Smstateen

<i>RISC-V "stimecmp / vstimecmp" Extension</i>	November 2021	Sstc
<i>RISC-V Vector Extension</i>	November 2021	Zve32x, Zve32f, Zve64x, Zve64f, Zve64d, Zve, Zvl32b, Zvl64b, Zvl128b, Zvl256b, Zvl512b, Zvl1024b, Zvl, Zv
<i>The RISC-V Instruction Set Manual Volume II: Privileged Architecture</i>	November 2021	Sm1p12, Ss1p12, Sv57, Hypervisor, Svinval, Svnapot, Svpbmt
<i>"Zfh" and "Zfhmin" Standard Extensions for Half-Precision Floating-Point</i>	November 2021	Zfh, Zfhmin
<i>"Zfinx", "Zdinx", "Zhinx", "Zhinxmin": Standard Extensions for Floating-Point in Integer Registers</i>	November 2021	Zfinx, Zdinx, Zhinx, Zhinxmin
<i>"Zhintpause" Pause Hint</i>	February 2021	Zhintpause
<i>The RISC-V Instruction Set Manual Volume I: Unprivileged ISA</i>	December 2019	A, D, F, RV32I, RV64I, Zaamo, Zalrsc, Zicsr, Zifencei
<i>The RISC-V Instruction Set Manual Volume II: Privileged Architecture</i>	December 2019	C, M, Q, Sm1p11, Ss1p11, Sv32, Sv39, Sv48