

RISC-V Technical Specifications

This page contains the single list of of all ratified technical publications.

ISA Specifications

Specification name	Version	Publish Date	RISC-V Community	Source Repository
The RISC-V Instruction Set Manual Volume I: Unprivileged ISA	20191213	Dec. 2019	Unprivileged Horizontal Committee	riscv/riscv-isa-manual
The RISC-V Instruction Set Manual Volume II: Privileged Architecture	20211203	Dec. 2021	Privileged Horizontal Committee	riscv/riscv-isa-manual

Note: Recently ratified extensions, but not yet included in the full specifications above, can be found on the RISC-V [Ratified Extensions](#) page.

Non-ISA Specifications

Specification name	Version	First Published	Last Updated	Description	RISC-V Community	Source Repository
Efficient Trace for RISC-V	2.0.3	June 2022	April 2024	Specifies the signals between the RISC-V core and the encoder, compressed branch trace algorithm, and the packet format used to encapsulate the compressed branch trace information to implement processor tracing.	SOC Infrastructure Horizontal Committee	riscv-non-isa/tech-trace-spec
RISC-V ABIs Specification	1.0	November 2022		Provides the processor-specific application binary interface document for RISC-V	Application & Tools Horizontal Committee	riscv-non-isa/riscv-elf-psabi-doc
RISC-V Advanced Interrupt Architecture	1.0	June 2023		Describes an Advanced Interrupt Architecture for RISC-V systems.	Privileged Software Horizontal Committee	riscv/riscv-aia
RISC-V External Debug Support	0.13.2	March 2019		Outlines a standard architecture for external debug support on RISC-V platforms.	SOC Infrastructure Horizontal Committee	riscv/tech-debug-spec
RISC-V Functional Fixed Hardware Specification	1.0.0	January 2024		Provides additional system specification for RISC-V systems which use Advanced Configuration and Power Interface (ACPI), specifically for some ACPI object fields of type "Resource Descriptor".	Privileged Software Horizontal Committee	riscv-non-isa/riscv-acpi-ffh
RISC-V IOMMU Architecture Specification	1.0.0	June 2023		Describes an Input-Output Memory Management Unit (IOMMU) that connects direct-memory-access-capable Input/Output (I/O) devices to system memory.	SOC Infrastructure Horizontal Committee	riscv-non-isa/riscv-iommu
RISC-V Platform-Level Interrupt Controller Specification	1.0.0	February 2023		Delineates the operational parameters for a platform-level interrupt controller on RISC-V.	Privileged Software Horizontal Committee	riscv/riscv-plic-spec
RISC-V Supervisor Binary Interface Specification	1.0.0	May 2022		Describes the RISC-V Supervisor Binary Interface, known from here on as SBI which enables supervisor-mode (S-mode or VS-mode) software to be portable across all RISC-V implementations by defining an abstraction for platform (or hypervisor) specific functionality.	Privileged Software Horizontal Committee	riscv-non-isa/riscv-sbi-doc
RISC-V Supervisor Binary Interface Specification	2.0.0	January 2024		Second publication of the RISC-V Supervisor Binary Interface specification. It added a debug console, system suspend, nested acceleration, steal-time accounting, PMU snapshot, and various error codes; relaxed counter width requirements on PMU firmware counters; reserved space for firmware events; and clarified several extensions.	Privileged Software Horizontal Committee	riscv-non-isa/riscv-sbi-doc
RISC-V UEFI Protocol Specification	1.0.0	May 2022		Details all new UEFI protocols required only for RISC-V platforms.	Privileged Software Horizontal Committee	riscv-non-isa/riscv-uefi

Note: If you do not see a specification in the above table, visit the RISC-V GitHub [riscv-non-isa](#) organization to see a complete list of all specifications which have been developed or are presently under development.

Compatibility Test Framework

The RISC-V Architectural Compatibility Test Framework Version 3 (RISCOF version 1.X) is now available.

This framework compares two arbitrary models against each other using a reference signature (one of which should be a reference model) and automatically selects tests according to the model configuration. Because the RISC-V ISA specification allows many architectural implementation choices, a tool (RISCV-CONFIG) has been created to describe implementation configurations. The RISCOF Framework uses RISCV-CONFIG to select and configure tests.

The current test coverage includes RV[32|64]IMCFD_Zb*_zK*_Zmmul_Zicsr_Zifencei (where * means a lot of sub extensions). Work continues to expand extensions supported and configurations covered.

More information can be found in the following locations

- Compatibility Test Framework (RISCOF) – [GitHub repository](#), [Documentation](#)
- Test Framework Configuration Tool (RISCV-CONFIG) - [GitHub repository](#), [Documentation](#)
- Architecture Compatibility Test suite (ACT) - [GitHub repository](#), [Test format specification](#)