All Specifications Under Development

Summary	Status	ISA or NON-ISA	In Fast Track?	GitHub	Extensions	Target BoD Ratification Approval	Updated
Address Range Invalidation	SPECIFICATION UNDER DEVELOPMENT	NON-ISA	Yes	https://github.com/riscv-non-isa/riscv-iommu-invalidation			May 10, 2024
Address Translation Cache Invalidation	SPECIFICATION INCEPTION	NON-ISA	Yes				Apr 26, 2024
Architectural Test User Specification	SPECIFICATION IN PLANNING	NON-ISA	No	https://github.com/riscv-non-isa/riscv-arch-test			May 08, 2024
Attached Matrix Extension	SPECIFICATION INCEPTION	ISA	No				May 08, 2024
Boot & Runtime Services (BRS)	SPECIFICATION IN FREEZE	NON-ISA	No	https://github.com/riscv-non-isa/riscv-brs		Nov 07, 2023	May 09, 2024
Brain Float 16 (BFloat16)	SPECIFICATION IN RATIFICATION-READY	ISA	Yes	https://github.com/riscv/riscv-bfloat16	Zfbfmin, Zvfbfmin, Zvfbfwma	May 30, 2024	May 09, 2024
CHERI	SPECIFICATION INCEPTION	ISA	No	https://github.com/riscv/riscv-cheri			May 08, 2024
Capacity and Bandwidth controller QoS Register Interface (CBQRI)	SPECIFICATION IN RATIFICATION-READY	NON-ISA	No	https://github.com/riscv-non-isa/riscv-cbqri		May 30, 2024	May 10, 2024
Composable Extensions	SPECIFICATION INCEPTION	ISA	No	https://github.com/riscv/composable-extensions			Apr 25, 2024
Confidential VM Extension (CoVE)	SPECIFICATION UNDER DEVELOPMENT	NON-ISA	No	https://github.com/riscv-non-isa/riscv-ap-tee			May 08, 2024
Confidential VM Extension (CoVE) with I/O	SPECIFICATION UNDER DEVELOPMENT	NON-ISA	No	https://github.com/riscv-non-isa/riscv-ap-tee-io			May 09, 2024
Control Transfer Records (CTR)	SPECIFICATION IN FREEZE	ISA	No	https://github.com/riscv/riscv-control-transfer-records	Smctr, Ssctr	Apr 25, 2024	May 07, 2024
Debug for Hardware Platforms	SPECIFICATION IN RATIFICATION-READY	ISA + NON-ISA	No	https://github.com/riscv/riscv-debug-spec/	Sdext Sdtrig	Jun 27, 2024	May 10, 2024
Dot-Product	SPECIFICATION IN PLANNING	ISA	Yes	https://github.com/riscv/riscv-dot-product			May 08, 2024
Double Trap	SPECIFICATION IN RATIFICATION-READY	ISA	Yes	https://github.com/riscv/riscv-double-trap	Ssdbltrp, Smdbltrp	Jun 27, 2024	May 01, 2024
Dynamic RVTSO	SPECIFICATION UNDER DEVELOPMENT	ISA	Yes	https://github.com/riscv/riscv-ssdtso	ssdtso		May 08, 2024
E-Trace Encapsulation	SPECIFICATION IN RATIFICATION-READY	NON-ISA	No	https://github.com/riscv-non-isa/e-trace-encap		Jun 27, 2024	May 10, 2024
Eliding Memory-Management Fences on Setting PTE Valid	SPECIFICATION IN RATIFICATION-READY	ISA	Yes	https://github.com/riscv/riscv-svvptc	Svvptc	May 30, 2024	May 10, 2024

External Debug Security	SPECIFICATION INCEPTION	NON-ISA	No	https://github.com/riscv-non-isa/riscv-external-debug-security			May 08, 2024
Extra Vector Carry-Less/Crypto Extensions	SPECIFICATION UNDER DEVELOPMENT	ISA	Yes	https://github.com/riscv/riscv-crypto/pull/362	Zvkgs, Zvbc32e	Jul 25, 2024	May 09, 2024
Fast Interrupts (CLIC)	SPECIFICATION IN FREEZE	ISA	No	https://github.com/riscv/riscv-fast-interrupt	Smclic, Ssclic, Suclic, Smclicshv, Smclicconfig	Jun 27, 2024	May 08, 2024
High Assurance Cryptography (HAC)	SPECIFICATION INCEPTION	ISA	No	https://github.com/riscv/riscv-hac			May 08, 2024
Input/Output Physical Memory Protection (IOPMP)	SPECIFICATION IN FREEZE	NON-ISA	No	https://github.com/riscv-non-isa/iopmp-spec		May 30, 2024	May 08, 2024
Instruction/Data Consistency	SPECIFICATION IN PLANNING	ISA	No	https://github.com/riscv/riscv-j-extension			May 10, 2024
Integrated Matrix Specification	SPECIFICATION INCEPTION	ISA	No	https://github.com/riscv/integrated-matrix-extension			May 08, 2024
Lightweight Isolation	SPECIFICATION INCEPTION	ISA	No	https://github.com/riscv/lightweight-isolation			May 08, 2024
Load-Acquire/Store-Release	SPECIFICATION UNDER DEVELOPMENT	ISA	Yes	https://github.com/riscv/riscv-zalasr	Zalasr		May 10, 2024
Load/Store Pair for RV32	SPECIFICATION IN PLANNING	ISA	Yes	https://github.com/riscv/riscv-zilsd	Zilsd	Sept 26, 2024	May 08, 2024
Memory Tagging	SPECIFICATION INCEPTION	ISA	No	https://github.com/riscv/riscv-memory-tagging			May 02, 2024
Nexus-based Trace (N-Trace)	SPECIFICATION IN FREEZE	NON-ISA	No	https://github.com/riscv-non-isa/tg-nexus-trace		May 30, 2024	May 08, 2024
Non-leaf Invalidation	SPECIFICATION UNDER DEVELOPMENT	NON-ISA	Yes	https://github.com/riscv-non-isa/riscv-iommu-invalidation			May 10, 2024
Packed Single Instruction, Multiple Data (SIMD)	SPECIFICATION IN PLANNING	ISA	No	https://github.com/riscv/riscv-p-spec	Zbpbo, Zpn, Zpsfoperand, P	Dec 29, 2023	May 01, 2024
Performance Events Specification	SPECIFICATION INCEPTION	ISA	No	https://github.com/riscv/riscv-performance-events			May 08, 2024
Platform Management Interface - RPMI	SPECIFICATION INCEPTION	NON-ISA	No	https://github.dev/riscv-non-isa/riscv-rpmi			May 08, 2024
Pointer Masking (J)	SPECIFICATION IN RATIFICATION-READY	ISA	No	https://github.com/riscv/riscv-j-extension	Smmpm Smnpm Ssnpm Supm Sspm	Jun 27, 2024	May 09, 2024
Post Quantum Cryptography	SPECIFICATION INCEPTION	ISA	No	https://github.com/riscv/riscv-pqc			May 08, 2024
Privileged Specification 1.13	SPECIFICATION IN FREEZE	ISA	No	https://github.com/riscv/riscv-isa-manual			May 01, 2024
Quality-of-Service (QoS) Identifiers	SPECIFICATION IN RATIFICATION-READY	ISA	Yes	https://github.com/riscv/riscv-ssqosid	Ssqosid	May 30, 2024	May 10, 2024
RAS Error Record Interface (RERI)	SPECIFICATION IN RATIFICATION-READY	NON-ISA	No	https://github.com/riscv-non-isa/riscv-ras-eri		May 30, 2024	May 09, 2024

RVA23	SPECIFICATION IN FREEZE	ISA	No	https://github.com/riscv/riscv-profiles/blob/main/rva23-profile.adoc	See the list of extensions at https://github.com/riscv/riscv-profiles/blob/main/rva23-profile.adoc#rva23u64-profile		May 08, 2024
RVB23	SPECIFICATION IN FREEZE	ISA	No	https://github.com/riscv/riscv-profiles/blob/main/rvb23-profile.adoc	See the list of extensions at https://github.com/riscv/riscv-profiles/blob/main/rvb23-profile.adoc#rvb23u64-profile		May 08, 2024
Resumable Non-maskable Interrupts	SPECIFICATION IN RATIFICATION-READY	ISA	Yes	https://github.com/riscv/riscv-isa-manual/blob/dfe0bbe540021ed3637c3ef0d76f05c780974eb6/src/rnmi.adoc#L135	Smrnmi	Jun 27, 2024	May 09, 2024
S-mode Physical Memory Protection (PMP)	SPECIFICATION IN FREEZE	ISA	No	https://github.com/riscv/riscv-spmp	Sspmp	Jun 27, 2024	May 08, 2024
Security Model	SPECIFICATION IN PLANNING	NON-ISA	No	https://github.com/riscv-non-isa/riscv-security-model			May 08, 2024
Semihosting	SPECIFICATION IN PLANNING	NON-ISA	Yes	https://github.com/riscv-non-isa/riscv-semihosting			May 10, 2024
Server Platforms	SPECIFICATION IN PLANNING	NON-ISA	No	https://github.com/riscv-non-isa/riscv-platforms			May 08, 2024
Server SOC	SPECIFICATION UNDER DEVELOPMENT	NON-ISA	No	https://github.com/riscv-non-isa/server-soc/			May 08, 2024
Shadow Stacks and Landing Pads	SPECIFICATION IN RATIFICATION-READY	ISA	No	https://github.com/riscv/riscv-cfi	Zicfiss, Zicfilp	May 30, 2024	May 02, 2024
Supervisor Domains Access Protection	SPECIFICATION UNDER DEVELOPMENT	ISA	No	https://github.com/riscv/riscv-smmtt	Smmtt		May 08, 2024
Trace & Diagnostic Data Transport Encapsulation	SPECIFICATION INCEPTION	NON-ISA	No	https://github.com/riscv-non-isa/e-trace-encap			May 08, 2024
Unified Discovery	SPECIFICATION UNDER DEVELOPMENT	NON-ISA	No	https://github.com/riscv/configuration-structure			May 08, 2024
Vector Crypto - all-rounds AES	SPECIFICATION IN PLANNING	ISA	No	https://github.com/riscv/riscv-crypto	Zvknf		May 10, 2024

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